ORIGINAL

CST THOR PROFESSIONAL COMPUTER SYSTEM TECHNICAL MANUAL.

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Keyboard circuits.

PCA's 4.03 ROM spec (partial)
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SECTION 1.00 QL Circuit board details.

1.01. The CST THOR Professional Computer system is based on an under/populated version of the Sinclair 'QL' personal computer circuit board. As several build levels of these exist, and the 'QL Technical manual' as published by Sinclair Research is generally inaccurate, it is intended to set out here an abbreviated description of the fundamental principles of operation of all versions likely to be encountered. It is assumed here that the ROM's or EPROM's installed in the QL board are of the correct type for the national character set required by the user of the machine, and also capable of correctly linking in the extensions to the operating system of the machine which turn the QL into a THOR.

1.02. The QL design is based upon the Motorola MC68008-8 processor which uses 32-bit data registers and data paths internally, like the 68000,68010 and 68012 members of the same family. The 68008 however truncates the external range of memory addressing by using only 20 address bits compared to 24 on the other parts, giving a maximum range of one Megabyte. This has no direct effect on the performance of the processor, other than to limit the amount of contiguous memory which can be accessed. The data path however is only implemented as 8 bits wide, forcing the processor to perform sequential accesses to transfer words or long words of data or programme code. These sequential accesses are performaed transparently by extra hardware on the 68008, which implements address line zero, to allow any single byte to be addressed. (This is done on the larger devices by decoding the upper and lower address strobe lines, which are replaced on the 68008 by a single address strobe). Naturally this type of sequential access has an effect on the overall speed of operation of the processor, and it is good programming technique to carry out as many operations as possible within the registers of the processor, using word length instructions, and keeping the number of long word accesses to a minimum. This has a direct bearing on the position of certain parts of the code within the system's memory-map, with the lowest 64K Bytes being specially valuable using the short addressing mode of the processor. At reset or power-on, the processor attempts to read two long words from the lowest addresses in the memory-map, these should contain the address of the restart entry point of the operating system code, and the address of a suitable memory location for use as the system stack. the next 254 long words are normally used for a table of addresses of the various service routines for Interrupts, trap calls, etc. For this reason this lowest 1K of the memory-map is usually implemented in RAM to allow these vectors to be easily changed, however the QL design uses 48K of ROM starting at the bottom of the memory-map to simplify the address decoding, and this adds an extra level

of indirection to the service code for all of these vectors, as they are pointing to fixed entry points in code elsewhere which then has perform a computed jump to the service routine required. This has an impact on the speed at which interrupts can be serviced, and in practice it is not possible to handle the double density floppy disc data rate by using interrupts or while they are enabled for system housekeeping purposes.

1.03. The ZX8301 ULA controls the overall timing of the processor and video diplay. A 15 MHz clock oscillator is incorporated, which uses an external Quartz crystal to produce a stable reference frequency from which all other timing intervals are sub-divided. The maximum pixel rate of the video display is 10 MHz, and 512 pixels are displayed in 51.2 microseconds as the trace scans the face of the picture-tube. The timing is padded out to 64 microseconds per line to allow the scan to return to the left hand edge of the tube, and data for the next line of pixels is then transferred. 256 lines of pixels are transferred to complete a single picture, and the overall time for this operation is then also padded out to allow the scanning beam to return to the top of the tube. The repetition rate for this entire picture is 50 Hz. In 4 colour mode each pixel is coloured according to the data contained in two bits of a byte transferred from memory, whilst in 8 colour mode 4 bits are used, reducing the number of pixels on a line to 256 for the same overall amount of memory (32 K) which is reserved for the video display.

The standard QL is fitted with 128K of RAM, which is made up of 16 64Kx1 parts. The ZX8301 controls these on a private data-buss, which allows them to be read at regular intervals as required by the video display, but this imposes a penalty in the access timing allowed to the CPU. The 68000 processors use an asynchronous interface to the outside world, and this means that access cycles can be of variable length. In the case of the standard memory of the QL, the minimum length of an access is 533 nanoseconds, but due to the video display taking priority some cycles will take up to 1.6 microseconds to complete. This has a marked effect on the speed of operation of programmes, as all of the internal memory is affected in the same way although only a quarter of it is actually used by the video display. The hardware is arranged in this way to keep down the costs and to automatically refresh the dynamic memory devices as the video data is read out. Finally the ZX8301 generates interrupts to the processor at the end of every picture scan, in order that the task-sequencing code in the operating system can be controlled.

1.04. The ZX8302 ULA is intended to handle a number of functions, and has several registers which can be set up to allow control of these. Firstly, this component handles the timing of the system reset line, which is delayed for approximately a second after power is applied to the

machine to ensure that the memory has been cycled enough times by the ZX8301 to be internally charged to a working state. Secondly a Crystal oscillator and binary counter is implemented, which counts in seconds to produce a readable clock for the machine. Third, the ZX8302 handles the outgoing data serialisation for the RS-232 ports, and the necessary handshaking inputs to control the sending process. Fourth, the ZX8302 controls the data serialisation and deserialisation of the network port (single line PNP open-collector pull-up type). Fifth, the ZX8302 controls the data transfers to and from the Microdrives, which are no longer implemented in the THOR machine. Fortunately removal of these devices fails-safe to the 'not found' condition as though no cartridge was inserted in the drive. Finally the ZX8302 handles serial data transfers to and from the 8049 Intelligent Peripheral Controller.

1.05. The IPC is a stand-alone mask-programmed microcontroller, which has it's own 11 MHz clock generator and ancilliary circuits to scan an 8 x 8 matrix of keyboard switches, two joystick ports (on the same matrix), control a 1 bit programmable noise generator, handle the incoming RS-232 lines asynchronously and buffer the data without disturbing the central processor, and communicate serially with the ZX8302. The keyboard scanning function is not used in the THOR, but without changing the masked code of this part, there is no way to actually disable this function without losing the RS-232 ports.

1.06. The Video outputs of the QL board are all based on the 3-bit RGB signals produced by the ZX8301. These are mixed with the synchronising signals to produce a composite monochrome signal with approximately 1 volt pk-pk data, sent direct to the monitor socket for a standard TTL input colour display, and also used to produce a modulated UHF signal without sound on channel 36 for a PAL standard television. Due to the bandwidth and picture convergence limitations of domestic televisions, a lower definition text mode is implemented for this situation, whilst monochrome and colour monitors should be able to display the high-resolution mode correctly. It is worth noting that most televisions and monitors expect a signal with only 40 to 48 microseconds of displayable video per line, and that the correct setting for the QL would allow the entire transmitted 'test-card' to be seen on the screen with a small black border all round it. Some televisions are designed to 'over-scan' to such a degree that it is not possible to reduce the width or height of the picture sufficiently to do this.

2.00. Startup sequence of standard QL.

2.01. The dynamic memory devices used in the QL design need to be cycled for a short period to build up their internal negative voltage supply before they will respond correctly to data-transfers. The Central processor unit also has a similar requirement, and to satisfy both of these needs, the reset and halt lines of the processor are held low for a period after the application of power to the machine. The processor also requires this type of delay if it is reset without removal of the system power, and so the system reset button connects in through the ZX8302, which duplicates the timing of the power-on reset. — Software reset instruction counts cycles to do the same thing.

2.02. As the processor comes out of reset, it attempts to read the lowest two long words of the ROM, to find the correct address of the system stack area and the entry point address of the operating system code. if anything upsets this sequence, then the ZX8301 will display the contents of the video memory (which depends on the individual memory devices in the board) and the machine may then take many different actions depending on the exact nature of the fault. The most common symptom is that the processor cannot understand the data or op-codes which it reads, and enters a loop trying to run the buss error trap, which it may also fail to read correctly. Ultimately the processor may stop due to a double buss error, and this can be identified by examining the function code pins of the processor and the static values on the address and data pins. — Halt line is Down. (o/p = 0)

2.03. If the restart vector is correctly read, the processor begins to execute the code at that address. This starts with a simple memory-test, which firstly checks the valid memory area at 64K intervals till it finds an address which does not give an alterable response. This is also affected by the non-use internally of the two most significant address lines from the processor, which limits the unexpanded hardware to a 256K memory-map. Subsequently the processor copies part of the lowest area of ROM into the RAM over and over again, until the highest populated RAM address as previously defined is filled. This gives the familiar screen pattern, which is actually slightly different depending on the version of ROM installed. As the pattern is being written, it is checked, and any failure to match with the correct value results in the video display area being filled with a code which is displayed as a white screen. The processor at this point stays in a tight loop of code re-drawing this value onto the screen.

2.04. Once the pattern has been written, it is verified, starting once again from the lowest address. Any failure to agree with the contents of ROM during this part of

(6 missing?)

the test causes the video display area to be filled with a code which actually produces a blank green screen, and likewise loops forever. Once the memory test is successfully completed, the code then sets up the ´Superbasic´ interpreter and tests for an expansion ROM in the slot at the rear of the QL. Should such a ROM be located, any banner message therein is displayed, and any extensions to ´Superbasic´ or ´QDOS´ are linked in. Following this, the main expansion area is similarily checked for additional ROM´s, and if found, then any messages are diplayed and the code linked in.

2.05. Finally the remaining portion of the ´prompt screen´ is drawn, allowing the user to decide which video format the machine is to be used in at that stage. The operating system then searches for a Microdrive cartridge in drive one, and if found, then searches for a file called ´boot´ on that cartridge. If found, any ´Superbasic´ programme in this file will be loaded and run, allowing the system to start up any desired sequence of operations. If no ´boot´ file is found, then the next stage is simply to enable the command line interpreter and wait for input from the

3.00 THOR hardware extensions to the QL.

3.01. The CST THOR professional computer syste contains many extensions to the hardware of a standard QL. Most of these have been proved in previous products from CST, but they are now implemented in different ways to take advantage of the reduction in redundancy possible by making a combined unit. The THOR hardware is constructed on three printed circuit boards: a small vertical piece which has no active components, and serves both as a mechanical link to the QL,and a suitable place to apply the power to the unit; a second small board which mounts horizontally, and may carry up to six EPROM´s, two of which contain CST´s proprietary additions to QDOS; and the main circuit board, which carries all of the active components and the various connectors needed by the circuitry. Each major division of this circuit board is described below.

3.02. A Programmable Array Logic device (PAL) is used to decode the system address lines, and generate the correct responses to the QL board whenever an access is made to areas outside the standard 256K memory-map. As the two most significant address lines of the processor are not connected on the QL main board, it is necessary to return a signal (referred to as DSMCL) to the QL to disable the ZX8301 whenever either of these address lines goes high. This is done by clamping the data strobe signal into the ZX8301 to the +5V rail using a transistor, and to avoid spurious effects, this must happen before the leading edge of the data strobe signal falls at the input to the ZX8301. A series resistor is fitted on the QL board to stop this clamp transistor holding the data strobe to other components high as well.

3.03. The THOR board has it´s own buffered data-buss, and the LS245 buffer is enabled from the PAL at the correct times. This buss is damped with 150 ohm series resistors to limit transmission line effects. The remaining sections of the PAL are used in conjunction with an LS74 dual flip-flop and the processor clock signal to produce the timing signals for the 512K of Dynamic RAM installed on the THOR board. Two LS258 multiplexer devices are used to apply A1 to A16 to the memory devices at the correct time, as row and column addresses. The memory is arranged in two banks of eight 256K x 1 devices, with alternate Bytes being addressed in alternate banks by feeding A0 to the PAL to simplify the address decode. The memory devices used are of the more expensive CAS before RAS refresh type, which allow for the refresh of the memory to be completely transparent. The PAL generates a refresh cycle for the memory every time the data strobe from the processor goes active. Only during an actual memory access is the refresh stopped. This method actually increases the power consumption of the memory devices

(? missing?)

slightly compared to a distributed refresh system, but this was judged to be of minor importance compared to the greater simplicity of the design.

3.04. Designed around the specification of the Alps Electronics ´IBM PC-AT compatible´ keyboard, the serial keyboard interface is implemented with a Motorola MC 6850 device, which is connected to the data and clock lines of the keyboard in such a way that data coming in from the keyboard is self-clocking, but the THOR can generate a clock pulse locally to shift the start bit out onto the data line whenever data is to be sent back to the keyboard, which will recognise the start bit on the data line and then generate the rest of the clock train. This process can go wrong when keyboard data is lost due to the keyboard being used during a data transfer to the floppy disc interface, when interrupts are disabled, and at these times, it is necessary to send a number of bytes to perform a reset at both ends of the keyboard cable. At present certain ´IBM compatible´ keyboards do not respond to the software of the THOR, and it may be necessary to alter the code or even the hardware if there is sufficient demand for these types of keyboard in the future.

3.05. The parallel printer port is implemented using part of a Motorola MC6821 device. This is a dual 8-bit device, and data to be sent to the printer port is written into the ´B´ side output register. The hardware is decoded to allow an access to a specific address to generate a strobe pulse for the printer port, and the timing of this is decided by the same circuit, using an LS 113, which slows down the central processor to generate a ´6800 peripheral´ type of access cycle for both the 6850 and the 6821. An input on the 6821 is used to read the status of the printer´s busy line, to sense the correct time for the transmission of the next byte of data. The interface is buffered with spare inverting elements from several devices on the board, and this means that data to be sent is actually inverted by the software before being written into the 6821 register.

3.06. The Mouse port is implemented using an LS74 flip-flop and part of the ´A´ side of the 6821. Information from the mouse is applied to the LS74, which then gives outputs indicating the direction of movement, and a pulse train for each axis. This is easier to handle than simply reading the 4 lines from the mouse and having to make decisions about directions in software. Three buttons are also supported on the Mouse interface.

3.07. Two lines from the remaining part of the ´A´ side of the 6821 are used to select drive 1 or two for the floppy disc interface, and these lines are ´OR´ed together as the Motor control line. The final two lines are used as side select, and double density enable, allowing the system to read single or double density discs from other

3.08. The floppy disc interface is implemented using a Western Digital WD1772 controller device, which has an internal digital data separator. It needs an external reference clock, and so an 8 MHz Crystal is used in a simple TTL oscillator to provide this. it is internally divided by the correct amount depending on the state of the double density enable pin. This interface is suitable for most 5 1/4" and 3 1/2" drives, but care should be taken that certain lines are not buffered and will not drive 150 Ohm terminating packs as fitted to many older drives.

3.09. The THOR system implements a battery-backed real-time clock, built around an Hitachi HD146818 device. This operates with a very low-powered crystal oscillator running at 32768 Hz, and will continue to operate for at least 14 days when the system is turned off. Operating from a re-chargeable 3.6V Ni-Cad battery, which is trickle-charged while the system is in use. To avoid upsetting the clock, a transistor is used to control the system's access during the power-up period. An input to the clock device senses the supply voltage, and when the battery is completely discharged this sets an internal flag at power-up , which is used to warn the system that the clock may not be accurate.

change to -
less than 1 volt.

SECTION 4.00. THOR startup sequence.

4.01. Initially the power-on startup sequence of the THOR system is identical to that of the standard QL computer, on which it is based. Once the sequence reaches the point described in section 2.04., where additional ROM's are searched for, instead of allowing the sequence to proceed as before, the user ROM area is checked at 16 K boundaries for the prescence of additional ROM's, until the first THOR ROM is located. This contains code which sets up the hardware of the THOR circuit board, but then it modifies the contents of the registers used in the search routine, such that the last three 16 K blocks are not accessed. This is done to prevent there being any uncontrolled accesses to the hardware area of the THOR board, which is transparently accessed as 'data space' at the same physical addresses as the highest ROM slot.

4.02. THOR ROM's from issue 4.00 onwards contain both a checksum verification routine, which should guarantee the integrity of the code therein; and a serial number/watermark identifying the machine as a THOR. This can only be checked by using a new trap-call in the extensions to the operating system. No attempt should be made to verify this by direct access to the ROM's as any access to this area will cause a hardware lock-up of the machine to occur.

4.03. The code contained in the initialisation sequence of the THOR ROM's sets up the different components on the board in a specific sequence. This sequence is of necessity complex because a number of the components are inter-dependant. In particular, a number of sections of the circuitry are capable of generating interrupts at certain times and these must not be enabled before the requisite service routines have been linked in to QDOS.

The Floppy disc system needs the undivided attention of the main processor during reads and writes, and therefore all interrupts are masked during disc accesses. During the startup sequence, the operating system performs a test to find the maximum stepping rate which the floppy drives will handle, and then tries to copy the directory of the first drive into memory, and searches for a 'boot' file. Until it is satisfied that none is present, the flashing cursor on the input line of the screen will not appear due to the system's temporary inability to handle interrupts from the keyboard. The cursor also disappears during subsequent disc accesses for the same reason. (Unlike the standard QL, the keyboard is not handled by a co-processor, and any keystrokes made during this period will be lost).

In single disc systems, a second drive is always checked for, and this check times out slowly due to the

non-detection of the index pulses from the second drive. If two drives are fitted, and neither has a disc installed, then this time delay is similar for each drive in turn. The quickest exit from this test is if both drives have a disc installed, but neither has a 'boot' file present. At this point the default device is changed to FLP1_.

4.04. The code then tests for the presence of the SCSI interface circuitry, and if it is installed, regardless of the presence of the actual winchester drive, the default device is set to WIN1_. This is carried out after the tests of the floppy disc system, in order that a system with a corrupted winchester 'boot' file can be diverted by inserting a floppy disc which itself contains a valid 'boot'.

The sequence is designed to allow the correct initialisation of the system with a new (unformatted) winchester drive, and it is not recommended that the system should be operated with the SCSI components installed, but without the actual drive. This does not cause any damage, just confusion over defaults. If the winchester is present, and correctly formatted, then the directory is copied into memory in the same way as for the floppy disc.

Certain operations may seem to take longer on the winchester disc, and this is due to the directory mechanism used. 16 K of memory is used for each directory present on the device, and due to the pre-sorting algorithm used when making directory entries, the full 16 K is scanned even if there is only a single entry. The SCSI data transfers are handled using interrupts, and this makes winchester accesses interleave with other interrupting events. Typically the keyboard will be useable during winchester accesses. The winchester system also performs 'write behind' to minimise the number of seeks made to the disc and this should be remembered when powering down the system, as the transfer of files may not be completed for a number of seconds.

4.05. The real-time clock is read during this sequence, and if the system has been powered-down for some length of time, then the message 'the clock has been reset' will be displayed on the screen. This is a warning that the date and time of the QL's clock will not have been set from the battery-backed one, and 'sdate' followed by 'set_clock' should be used as detailed in the owner's manual. Under normal circumstances, the QL's clock will be set to the same date and time as the battery_backed unit, and no warning message will appear.

4.06. The keyboard interface is enabled at this point, and this works by forcing the values of any keystrokes into the buffer previously used by the 8049 processor of the QL. This is done for compatibility with existing software, as

certain applications packages, and the 'alt-enter' keystroke sequence (restore previous line) directly read from this buffer.

4.07. Once the type of storage devices present has been identified, the code re-joins the standard QL power-up sequence, and performs an 'lrun' command on the 'boot' file if found on the default device.

7.00. Test and maintenance of the THOR system.

7.01 The THOR professional computer system is based on the main circuit-board of the Sinclair QL computer, with numerous additions to both hardware and software. As the QL circuit-board is mostly unchanged (issues 5 to 7 with JS ROM´s), it can be tested in isolation from the remaining components of the THOR. It is only necessary to provide the board with a regulated 5 Volt supply, and a standard QL membrane keyboard in order that the normal QL test procedures can be carried out.

If necessary, Microdrives can be used to assist in the rapid loading of test software, but unmodified microdrives will not function if connected, as they require an unregulated 9 Volt supply. The THOR system uses the old 9 Volt output pins of the expansion connector to feed it´s 5 Volt supply on to the circuit-board, and the 9 Volt and 5 Volt traces on the board are connected together. Microdrives can be modified to operate with this 5 Volt supply by removing their 7805 voltage regulators and linking the two outer pin-positions together on the board.

If no other means of powering the QL circuit-board is available, it is possible to make an adapter which transfers power from the THOR chassis to the QL board via a backplane type DIN 64-way connector on flying leads.

7.02. The QL circuit-board contains several custom logic devices, and a mask-programmed microcontroller. Two of these devices are generally the most likely components to cause problems with an established QL board. The Video Controller device (ZX 8301)is easily damaged by outside influences, as it drives the RGB video monitor directly. If the video monitor used is not separately grounded, and is then plugged into the THOR system whilst still carrying a static charge, the device will very often be damaged as the static will discharge through whichever pin makes contact first. The output drivers of the device are only specified against temporary short-circuits to ground or the 5 Volt supply, and as little as 10 Volts will cause permanent damage.

7.03. Symptoms vary, depending on the exact damage done to this part. In general the system will power-up with a blank white screen, with or without synchronising pulses for the monitor, but there are also failure modes where the screen carries a fixed pattern, or one or more colours fail to appear. Normally when a blank white screen appears, the system never comes out of reset, as the white screen is an indication of total RAM failure. This is not totally surprising, as the RAM timing is controlled by the Video Controller, and the reset sequence tests all RAM before

doing anything else. The modes with a pattern displayed on the screen are usually due to internal short-circuits between address lines inside the Video Controller (a similar situation arises when an external short is present in the machine), but the timing chain is still intact. The display represents the power-on state of the memory devices in the video display area, which the processor is unable to set to white due to the address-line fault. Missing colours are simpler to diagnose, as the rest of the system still works correctly.

7.04. The ZX8302 communications controller is also prone to failure due to the number of connections which are brought out to the outside world. Firstly the external interrupt line of the expansion connector is fed directly to this device, and unfortunately it is on the pin next to the -12 Volt supply. A bent pin on the expansion connector is all that is needed to destroy this device, and although this should not happen internal to the THOR machine, it can still happen to the connector in the expansion slot at the rear. A variety of symptoms can follow from damage to this component, with the most common being the sudden 'slowing down' of certain machine functions due to the overhead involved in servicing a permanent but unidentifiable interrupt.

Other lines on this device which appear externally are the handshake lines of the serial ports, and again a wide variety of faults can occur as a result of damage to this component. Failure to transmit to a serial device, 'not found' messages when the device is actually ready, etc.

7.05. Naturally over a period of service, there are many thinges which can cause problems with a system as relatively complex as the QL circuit-board, however, fortunately there seems to be a relatively low failure rate on the major components used, apart from the situations described above. The Central processor device (MC68008-8) is prone to damage from external hardware, especially when it is remembered that all of the address and data lines of the system originate from this part, and are all unbuffered at least as far as the expansion connector.The THOR hardware does buffer the data lines, but they represent only a small group, and it is likely that they will also be unbuffered on any add-on card.

Peripherals should always be connected when the system power is switched off, and wherever practical all elements of the system should be independantly earthed to remove the risk of damage from static charges. Always use a good mains distribution block, and make sure that the mains leads are the FIRST thing which you plug in when setting up the system. This guarantees that any static charge will dissipate safely through the earth wiring, and that there will be zero potential difference between items which are to be connected

7.06. Memory faults on the QL are of two kinds; firstly, there are those which are induced by the Video Controller device, when it is itself faulty; secondly there are genuine memory device failures. The first category are easily solved, as they disappear when the Video Controller device is replaced. The second type are more difficult to trace, in general the more catastrophic the fault, the easier it is to locate. It sometimes helps to hold the QL reset button in when powering up the board, as the pattern then displayed is the natural reset state of the memory devices.

Thin vertical lines on the screen at regular intervals can indicate specific bits faulty in the RAM, but further diagnosis is assisted by the QL's memory test sequence, which stays in a loop of code, writing a known value to the screen memory at successive locations when it fails. It is necessary to investigate the individual memory devices using an oscilloscope, to search for unusual waveforms.

7.07. Further investigation of the QL board is likely to be a lengthy business, with intermittent faults being particularily difficult to locate. Without test firmware in ROM, a digital storage 'scope, or a logic analyzer, it will often be simpler to obtain a service-exchange replacement for the QL circuit-board. If you return a faulty board under these circumstances, please give as full a description as possible of the problem, as it may not re-appear immediately when the board is being repaired by CST.

7.08. The THOR main board is currently built using a relatively large number of discrete devices, as this was judged to be the most economical method for production quantities below 1000 per month. The largest category of faults encountered so far is due to the low-volume hand-assembly techniques used, and due to the stringent quality-control checks, these rarely leave the factory uncorrected.

There is presently insufficient data to suggest that any specific failure pattern has occurred in the field. Whilst this is reassuring in general terms, it has the unfortunate side-effect that every fault is likely to be a new one, and therefore all the more difficult to track down.

7.09. The larger integrated circuits, and the custom PAL devices are all installed in sockets to reduce the chances of damage from static charges while the boards are being handled in the factory. There is no reason to suppose that they are more likely to fail than the other components, and they should not be removed from their sockets without proper anti-static precautions being taken. It is

occasionally found that atmospheric pollutants can cause problems with the sockets, but careful removal and re-insertion of the components would seem to be a sufficiently good method of removing any surface contamination. Spray-cleaners should not be used, as they often leave an oily residue on the surface of the circuit-board. This can become a sticky mess with small bits of dust and dirt mixed in over a period of time, and the added capacitance of such a deposit has been known to upset the operation of computer systems.

7.10. The THOR hardware can fail in a variety of ways, but in general it is unlikely that any of these will stop the QL board from operating normally. Memory faults can stop the power-on sequence being completed, but applying a temporary ground to pin 9 of IC 4 the main PAL device, will disable the THOR´s RAM completely. If this allows the power-on sequence to complete (with 128 K of RAM), then a memory test can be carried out from superBASIC, with the ground removed, to locate the problem.

7.11 Generally it will be found that the circuitry used on the THOR main board is sufficiently modular that specific faults can be rapidly diagnosed within the small area of circuitry associated with particular functions. However, there are faults which can cause the THOR hardware to stop the QL board operating correctly, and among these the most likely is for a faulty component to either short two signals together internally, or to ignore an input. Both of these conditions are likely to stop the power-on sequence at some indeterminate point, and without the use of an oscilloscope or logic-analyzer to examine the state of all relevant signals at the central processor, it is very difficult to make an accurate diagnosis. Typically a processor cycle will start by placing a valid address on it´s outputs, and then activating the address and data strobe lines (active low). If the address is in THOR board space, then IC4 the main PAL should take pin 14 high, activating the DSMCL line via Q1. Pins 12 and 13 should be in the appropriate state for the actual address present, and either DTACK or VPA should be activated to complete the cycle. Usually neither of these signals will occur, holding the processor from completing the cycle. Depending on the specific address, the state of the logic chain can be followed until the reason for this inactivity is located.

7.12 The second class of fault likely to be encountered is that which does not complete the power-on sequence, but which appears to be executing code. Again the exact hardware state must be checked, but when DSMCL, DTACK, and all address and data lines appear to have normal signal levels on them, it is likely that one of the peripheral devices is not returning the expected value when polled, and the processor is running a loop of code which is waiting for

the correct state to occur. The chip-select inputs of the various devices can be examined to find the one primarily involved, and other inputs to that device can be examined to locate any unusual signal conditions.

Alternatively, it is likely that at least one of the processor pins will show an unusual signal level, and it may be necessary to follow the tracks on the circuit-board to locate the reason for this irregularity. Bear in mind that the RAM has it´s own local data buffer, and that a short between lines on the RAM side of this will just look like identical data on two lines at the processor. Equally, the read/write line is buffered independantly for the RAM and all other devices. The signal may be present at the CPU, but not at the RAM or the other devices.

7.13. The RAM array has it´s local address lines multiplexed in IC´s 16 and 17, and it may not be obvious that the address lines may be perfectly alright at the processor, but shorted together, open-circuit between memory devices, or not being multiplexed at all. In normal operation, the main PAL device outputs two types of timing pulses on pins 16, 17, 18, and 19, to control the RAM during normal access cycles and refresh only cycles. It may be worth disabling the RAM as described in section 7.10., to stabilise these signals to the refresh only type when searching for a RAM fault.

SECTION 6.00. Hardware upgrades.

6.01. The basic production specification of the THOR computer system includes a single 3 1/2" 80 track double sided double density floppy disc as the data storage device. This can be supplemented by the aaddition of a second identical drive, a second non-identical drive (if required for media compatibilty with other systems), or by fitting the SCSI interface components and a 20 Megabyte 3 1/2" winchester drive.

6.02. Access to the internal components of the THOR system is obtained by removing the four M3 screws which secure the top cover, and then sliding this cover forwards until it is free of the chassis. This may be made easier if three of the four screws securing the plastic feet of the machine are slackened first. The screw holding the rear left-hand foot should not be slackened, as it is used internally to secure the main printed-circuit-board to the chassis.

6.03. The standard assembly arrangement is that single floppy versions of the system have the drive (selected as drive 1) installed in the rightmost slot of the chassis so that when a winchester drive is installed, it will be fitted into the central position.

When a second floppy drive is installed, placing it into the central position in the chassis would make the logical sequence of drive-numbering incorrect, and it is recommended that either the original drive is moved to the central position, with the new drive (selected as drive 2) installed at the right-hand side, or that the selection links on both drives are adjusted to place drive 1 in the central position.

6.04. The exact details of this link-adjustment procedure vary from one make of drive to another, so it may be necessary to consult the drive manufacturers information to carry this out correctly. In most cases, there will be a double row of small pins sticking up from the surface of the circuit-board of the drive, and there will be one or more push-on bridging plugs already installed on these pins. It is likely that a legend will be present on the circuit-board, with DS0, DS1, DS2, DS3, and possibly HM, HS, DS, or MX markings. The THOR software uses drive 1 and 2 to identify the devices, but the actual drives use DS0 for drive 1, and DS1 for drive 2.

Install the bridging plug across the correct pair of pins before installing the drive(s). The other selections are less important, as they will only affect the internal time-delays of the drive during the selection process. The THOR software should cope with any setting you are likely to

encounter. If you have problems, refer to the drive manufacturers data-sheet.

6.06. Certain drives have their interface circuitry built with C-MOS devices to reduce power consumption for portable computer systems; the THOR circuitry may not operate correctly with this type of drive, especially if a mixture of drives is installed in the machine. It may also be desired to extend the connections outside the THOR case to connect to existing drives (possibly 5 1/4"), and it must be made clear that this will only operate correctly if the length of the cable is kept down to less than 1 Metre, and the drives do not have terminating resistors fitted.

6.07. All machines are shipped with a power cable for two floppy drives installed, it is necessary to replace this with the alternative part for the winchester upgrade. These cables use insulation displacement connectors, and care must be taken not to loosen the wires as they are handled. These cables are all fitted in identical positions, and the only difficulty likely to be encountered is the removal of the connector from the small vertical circuit-board, which has locking clips behind it. This may be made easier if the QL circuit-board is removed first (3 screws), to improve access.

6.08. Single floppy machines are shipped with a ribbon cable with only two connectors installed. It is necessary to replace this with a three-connector version for the dual floppy machines, or to add the winchester cable for SCSI machines. These cables are fitted by pushing the connectors on to pins on the drives and on the main circuit-board, and polarity is important. The dual floppy cable has an identical section to the single floppy cable, and this should be installed in the same position. The additional connector can then be fitted to the second drive, with the connector the same way round as that on the first drive. The winchester cable will only fit one way round, as there are different numbers of pins on the two connectors. It is important to check that there is not a twist in the cable, as this will stop the system completing the power-on reset sequence.

6.09. All necessary hardware (bolts, spacers, cables, etc) will be provided in upgrade kits supplied by CST, and installation instructions will also be provided where necessary.

It seems likely that a number of dealers will want to carry out their own upgrades, and with this in mind full details of the parts needed are included in the main parts-list at the rear of this manual. CST will not accept liability for any consequential loss or damage caused by the installation of dealer-supplied upgrades to the THOR system.

Certain items will only be available from CST, or their agents, most notable of these is the winchester upgrade kit, which includes the Custom PAL device for the SCSI interface. The price of these components also inherently includes a licence fee for the use of the proprietary SCSI interface drivers provided in the THOR ROM's, and the winchester utilities disc which will be shipped with this kit.

6.10. The upgraded THOR system should be given a full functional test, including the formatting of a winchester drive if installed. CST has test software available to dealers to simplify this process, but it is preferable that this test is carried out before the cover is re-fitted, and then repeated after several hours of running with the cover installed. The power-supply of the THOR system is specified for the fully_upgraded system; however the power consumption is doubled when the winchester drive is installed, and this will result in a higher operating temperature than systems which only have floppy drives. This increase in temperature may show up faults which have previously gone unnoticed.

5.00. Optional SCSI Interface.

5.01. The THOR computer system has provision for a Small Computer Systems Interface (SCSI) port to be installed on the main circuit-board. This hardware is able to interface to SCSI devices using the 'single master' system, no provision is made for bus arbitration between intelligent peripheral devices to take place.

5.02. The SCSI standard defines voltage levels, pin connections, and minimum timings of all signals used by the interface circuitry. However, the system is asynchronous in operation, with no maximum time limits being imposed on many of the operations of the interface. The highest speed of data transfer using this type of interface requires DMA hardware, but this is not implemented on the THOR.

5.03. The hardware consists of 4 Integrated circuits which may be field-installed into sockets provided on the circuit-board. Several passive components are also required, but it has been decided that these will be incorporated into the assembly of all issues of the circuit-board at the factory, to avoid the need to remove the circuit-board from the chassis during conversion.

5.04. The Components required for the SCSI interface are IC.11 (74LS05) a hex open collector inverting buffer; IC.12 (74ALS638) an inverting octal tri-state line driver/receiver; IC.13 (PAL 16 L8) a programmable logic device with proprietary design to control the interface timing; and IC.15 (74LS245) an octal bidirectional three-state line driver. These parts will be available in the THOR spares kit from CST.

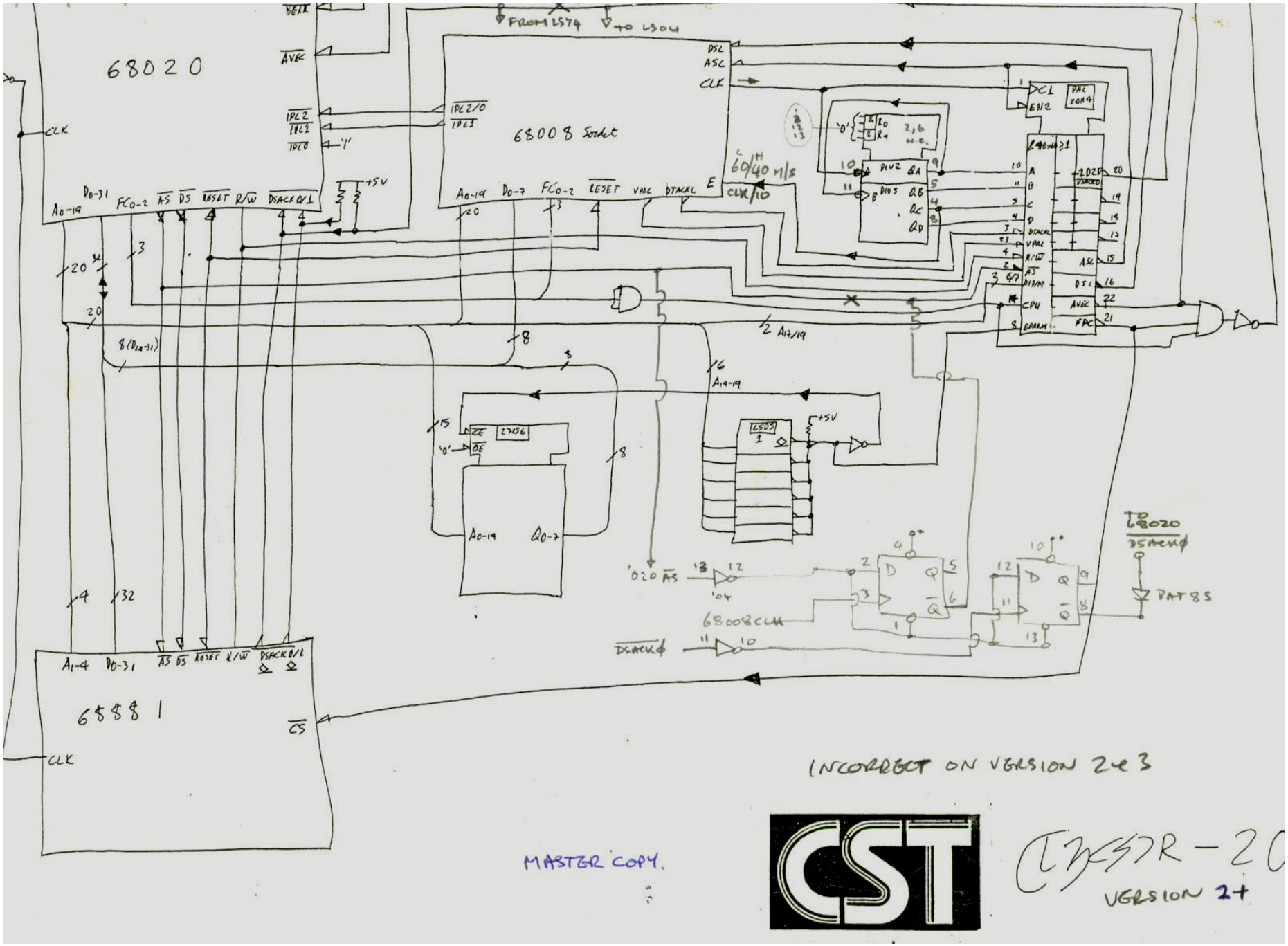
5.05. The SCSI standard also defines the 'Common Command Set' or CCS, which is a small kernel of the possible instruction codes available. This is intended to persuade different peripheral manufacturers to use the same group of commands uniformly, to allow a greater degree of interchangeability between their products. However at present this is not the case with 20 Megabyte winchester discs, and the THOR software presently supports only the RODIME RO652 drive.

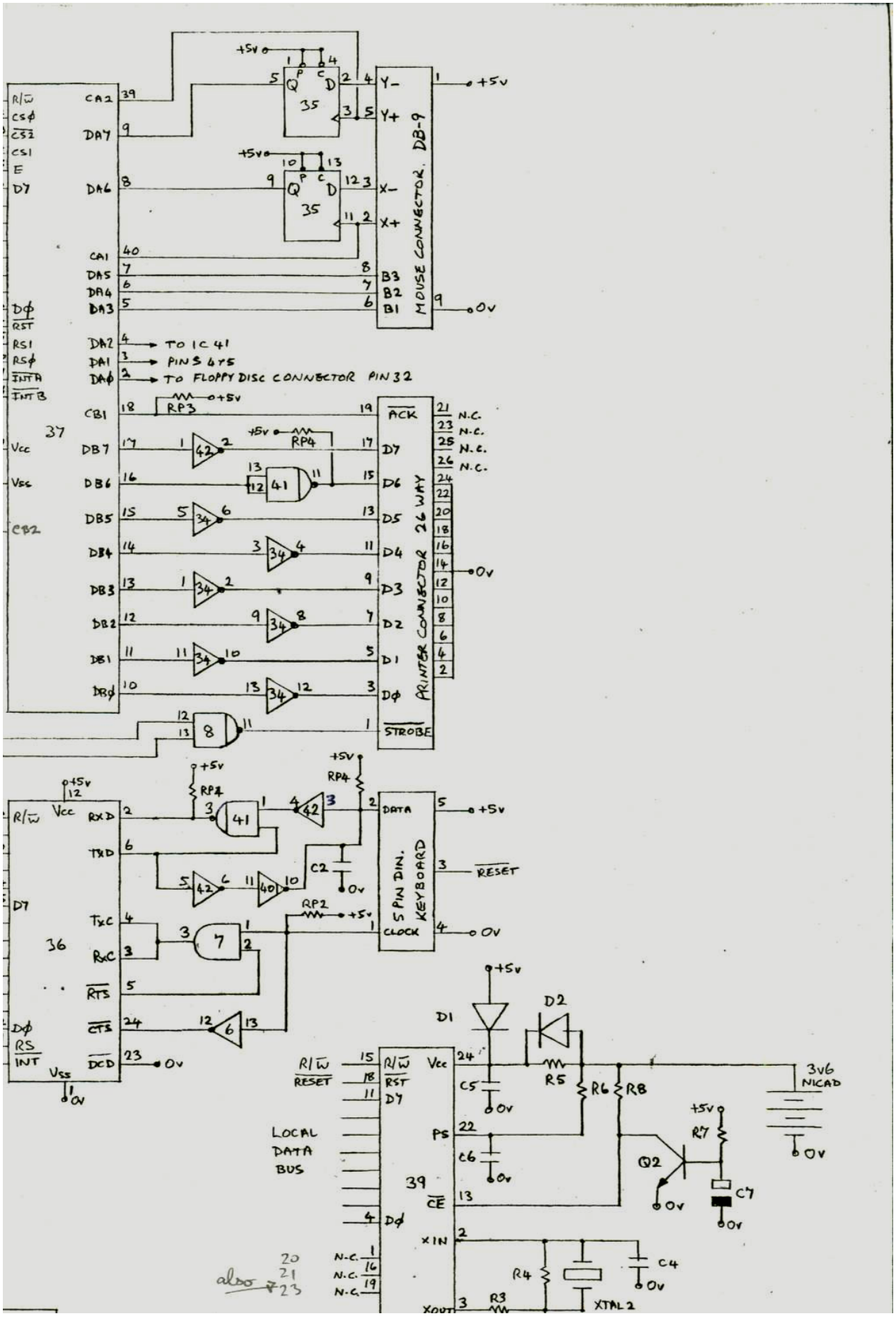
The driver software has presently been left so that up to eight devices can be adressed, however they must all be the same type. It is possible that the code in later issues of the THOR ROM's will be extended to allow the use of other specific devices on this interface.

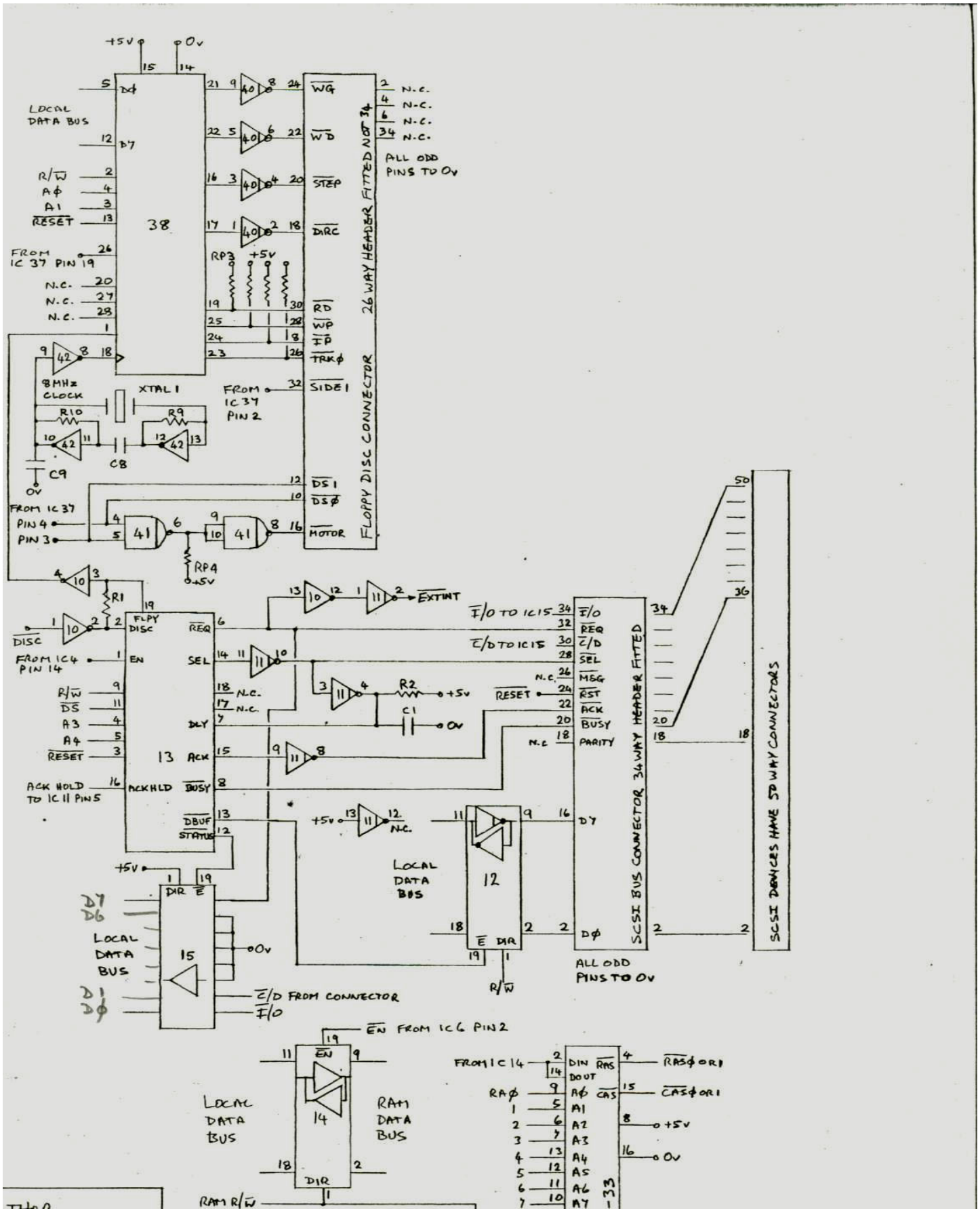
5.06. The SCSI interface as implemented on the THOR computer is normally connected to an internal device, powered from the internal voltage supplies. However access has been provided to the connector through a slot at the top

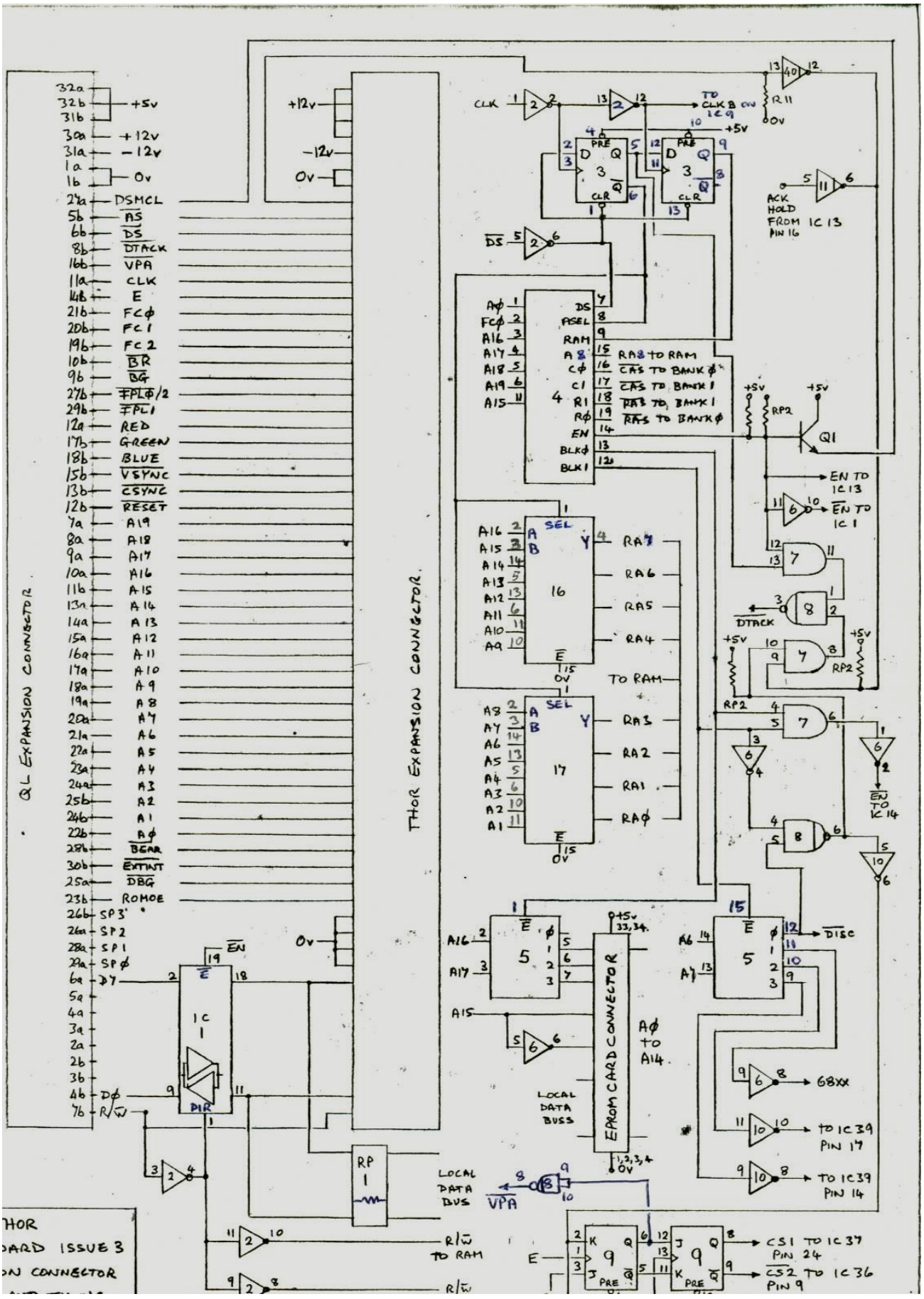
of the rear panel of the machine, so that externally powered devices can be connected. If this is done, it is necessary to arrange that only the devices on the ends of the ribbon cable are fitted with terminating resistor networks, and that the device on one end is no more than 150 mm away from the connector on the main circuit-board. The interface uses the single_ended signal convention, and there is therefore a limit of 3 Metres maximum between the first and last devices on the cable. Devices should all be of this type; balanced line devices will not work.

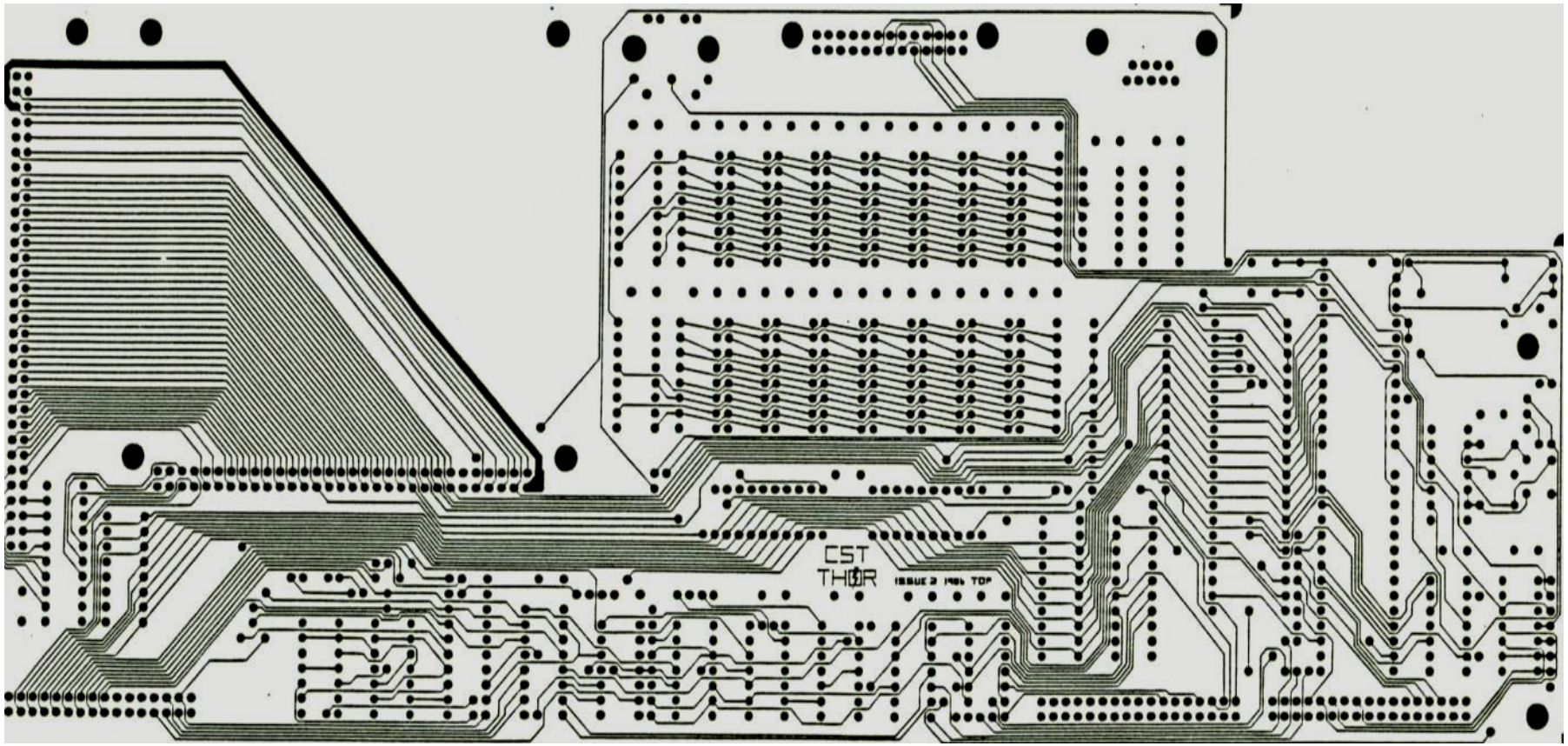
5.07. The winchester disc is formatted in blocks of the standard QL size (512 bytes), and block transfers are initiated by interrupts from the interface circuitry. However these block transfers are interruptable, and therefore other operations can proceed while data is transparently transferred at a slightly reduced speed. This compares favourably with the floppy disc interface, which has to mask all interrupts and poll the disc controller device

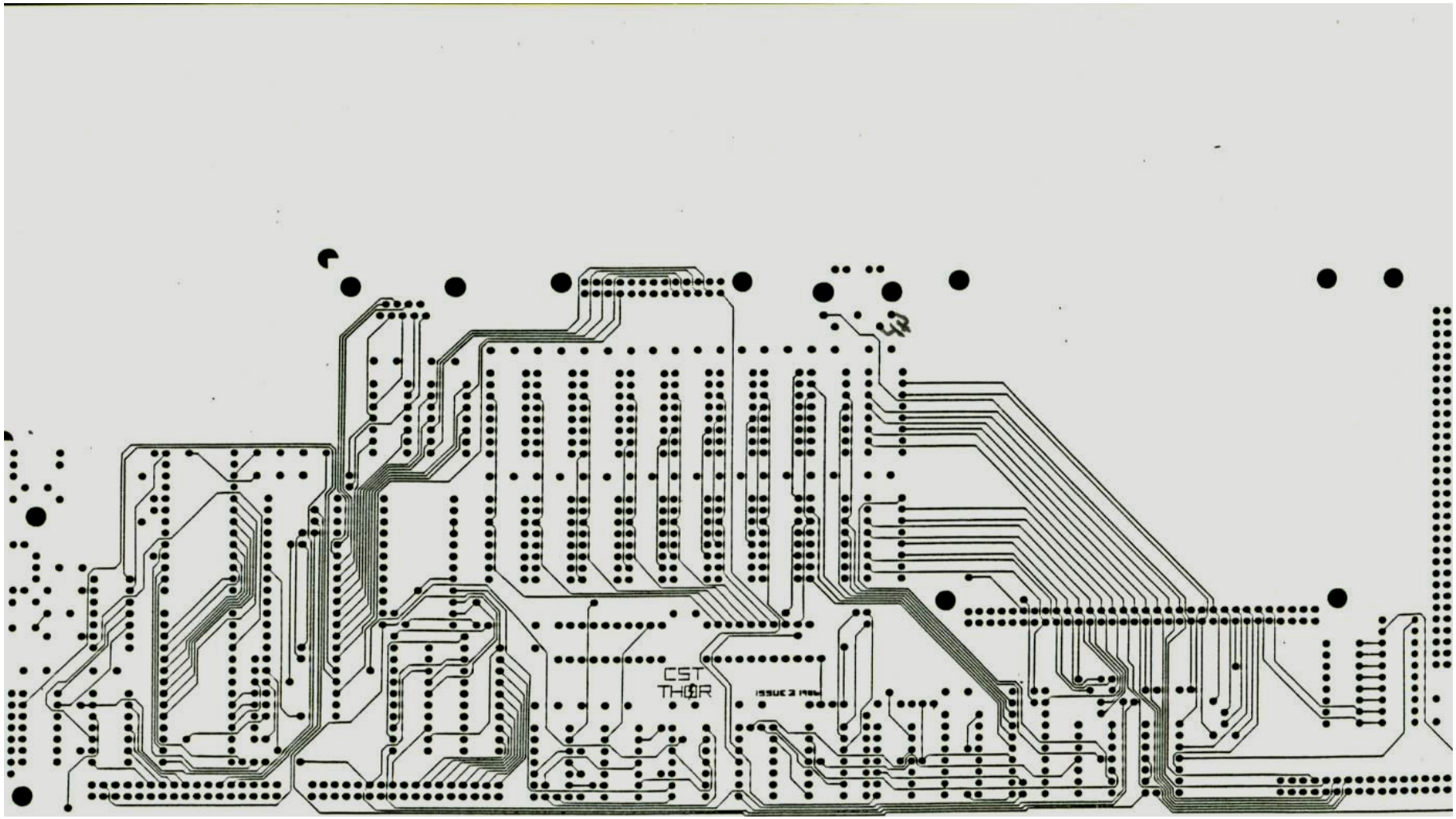

68020
68008 Socket
FROM LS74
TO LS04
CLK
AVEC
IPL2
IPL1
IPL0
IPL2/0
IPL1
'1'
+5V
A0-19
D0-31
FC0-2
AS
DS
RESET
R/W
DSACK0/1
DSL
ASL
CLK
E
60/40 M/S
CLK/10
PAL 20R4
CL
EN2
PLV2
PLV8
QA
QB
QC
QD
A
B
C
D
DTACK
VPAL
R/W
AS
DISAB
CPU
EPROM
DSL
ASL
AVEC
FPC
DSACK0
DSACK1
2764
OE
CE
LS05
A0-19
Q0-7
A17/19
A19-19
'020 AS
'04
68008CLK
DSACK0
DAT8S
TO 68020 DSACK0
A1-4
68881
CS
INCORRECT ON VERSION 2 & 3
MASTER COPY.
CST
CPUSTR-20
VERSION 2+

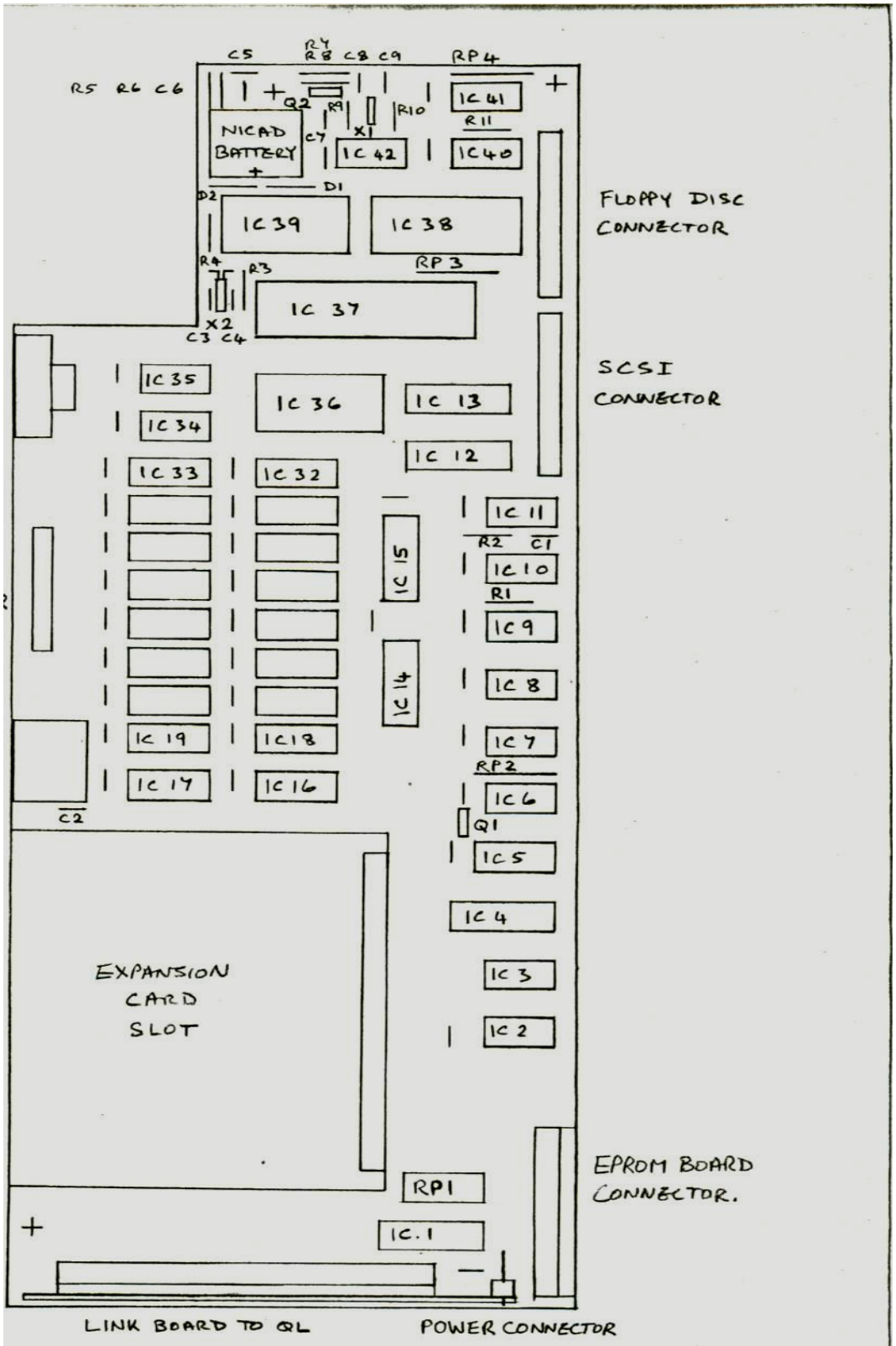

MOUSE CONNECTOR. DB-9
PRINTER CONNECTOR 26 WAY
5 PIN DIN. KEYBOARD
TO IC 41
PINS 4 & 5
TO FLOPPY DISC CONNECTOR PIN 32
LOCAL DATA BUS
3V6 NICAD
XTAL 2
+5v
0v


+5V
0V
LOCAL DATA BUS
R/W
AØ
A1
RESET
FROM IC 37 PIN 19
N.C.
N.C.
N.C.
38
RP3
+5V
WG
WD
STEP
DIRC
RD
WP
TRKØ
SIDE1
FROM IC 37 PIN 2
8MHz CLOCK
XTAL 1
R10
R9
C8
C9
FROM IC 37 PIN 4
PIN 3
DS1
DSØ
MOTOR
FLOPPY DISC CONNECTOR 26 WAY HEADER FITTED NOT 34
N.C.
ALL ODD PINS TO 0V
RP4
R1
DISC
FLPY DISC
EN
SEL
DLY
ACK
ACKHLD
BUSY
DBUF
STATUS
REQ
EXTINT
I/O TO IC15
C/D TO IC15
R2
C1
RESET
ACK HOLD TO IC11 PIN5
DIR
E
LOCAL DATA BUS
C/D FROM CONNECTOR
I/O
SCSI BUS CONNECTOR 34 WAY HEADER FITTED
I/O
REQ
C/D
SEL
MSG
RST
ACK
BUSY
PARITY
ALL ODD PINS TO 0V
SCSI DEVICES HAVE 50 WAY CONNECTORS
EN FROM IC6 PIN2
RAM DATA BUS
RAM R/W
FROM IC 14
DIN
DOUT
RAS
CAS
RASØ OR1
CASØ OR1
-33


QL EXPANSION CONNECTOR
THOR EXPANSION CONNECTOR
+5v
+12v
-12v
0v
DSMCL
AS
DS
DTACK
VPA
CLK
E
FC0
FC1
FC2
BR
BG
FPL0/2
FPL1
RED
GREEN
BLUE
VSYNC
CSYNC
RESET
A19
A18
A17
A16
A15
A14
A13
A12
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
BGACK
EXTINT
DBG
ROMOE
SP3
SP2
SP1
SP0
D7
D0
R/W
IC 1
DIR
EN
RP 1
TO CLK B ON IC 9
R11
ACK HOLD FROM IC 13 PIN 16
RA8 TO RAM
CAS TO BANK 0
CAS TO BANK 1
RAS TO BANK 1
RAS TO BANK 0
RP2
Q1
EN TO IC 13
EN TO IC 1
EN TO IC 14
DTACK
RA7
RA6
RA5
RA4
TO RAM
RA3
RA2
RA1
RA0
EPROM CARD CONNECTOR
A0 TO A14
LOCAL DATA BUS
DISC
68XX
TO IC 39 PIN 17
TO IC 39 PIN 14
VPA
R/W TO RAM
CS1 TO IC 37 PIN 24
CS2 TO IC 36 PIN 9


CST
THOR


CST
THOR



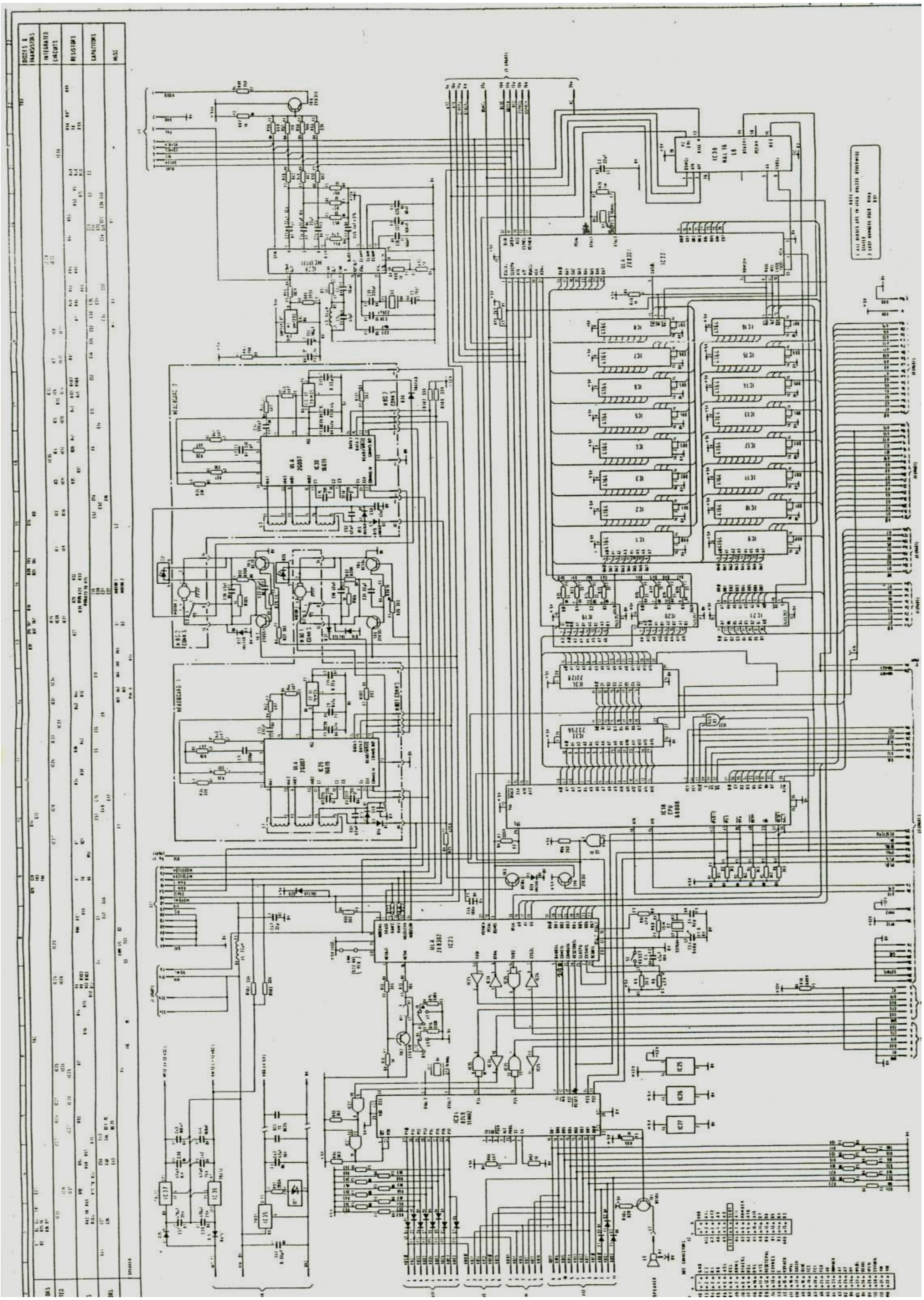
MAIN CIRCUIT BOARD ISSUE 3. AUGUST 1986.

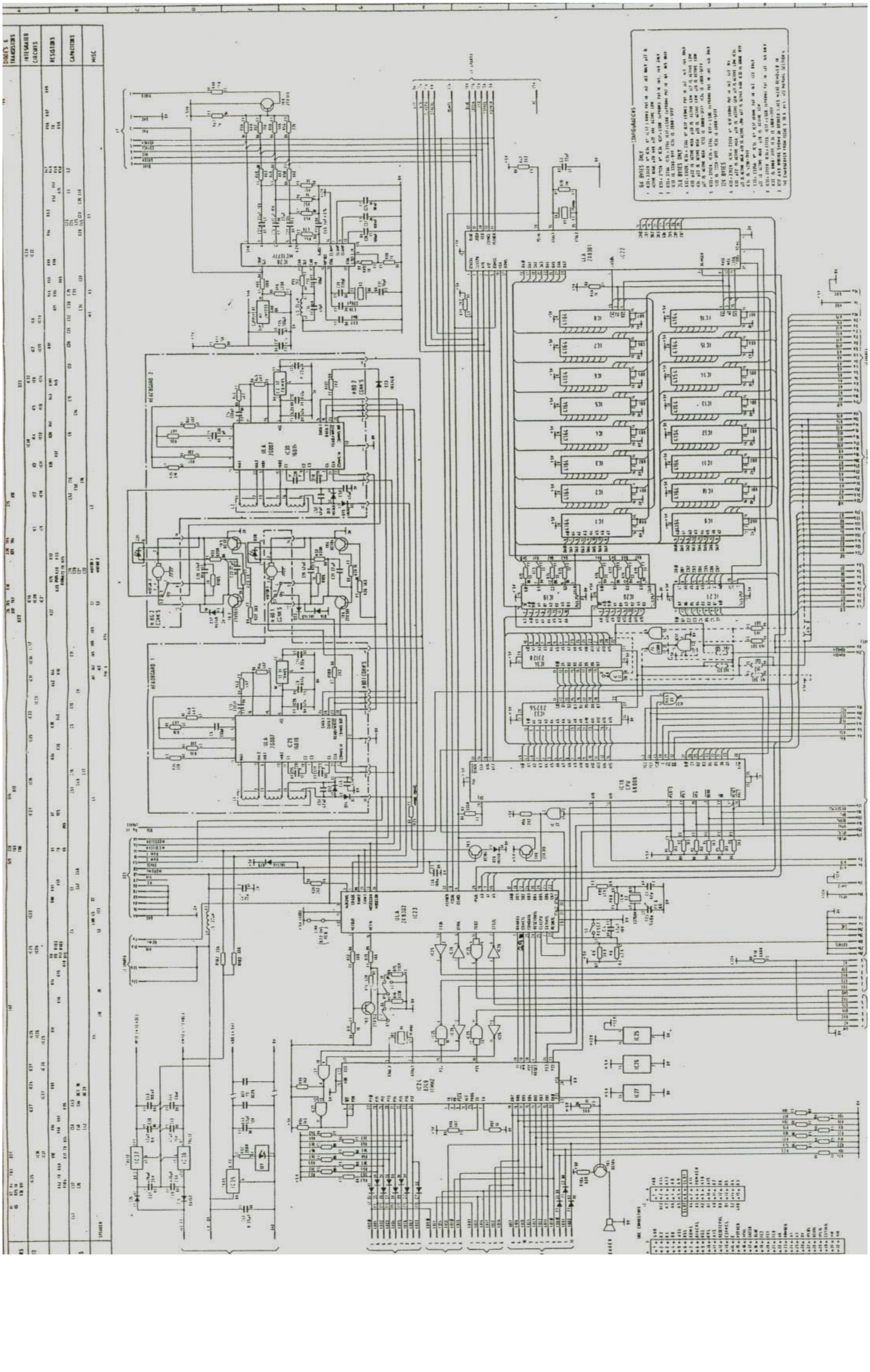
D CAPACITORS ARE FOR DECOUPLING ONLY

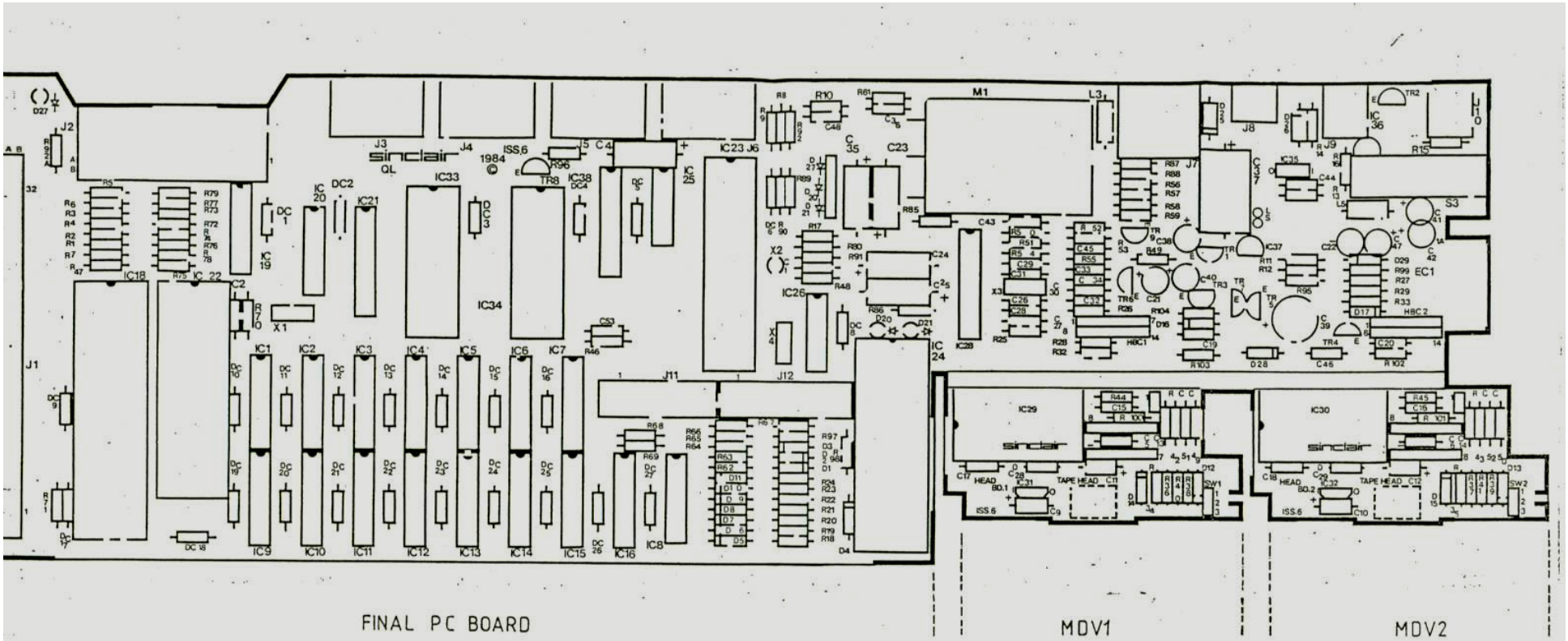
:7 ARE CURRENTLY MOUNTED ON THE SOLDER SIDE.

AL

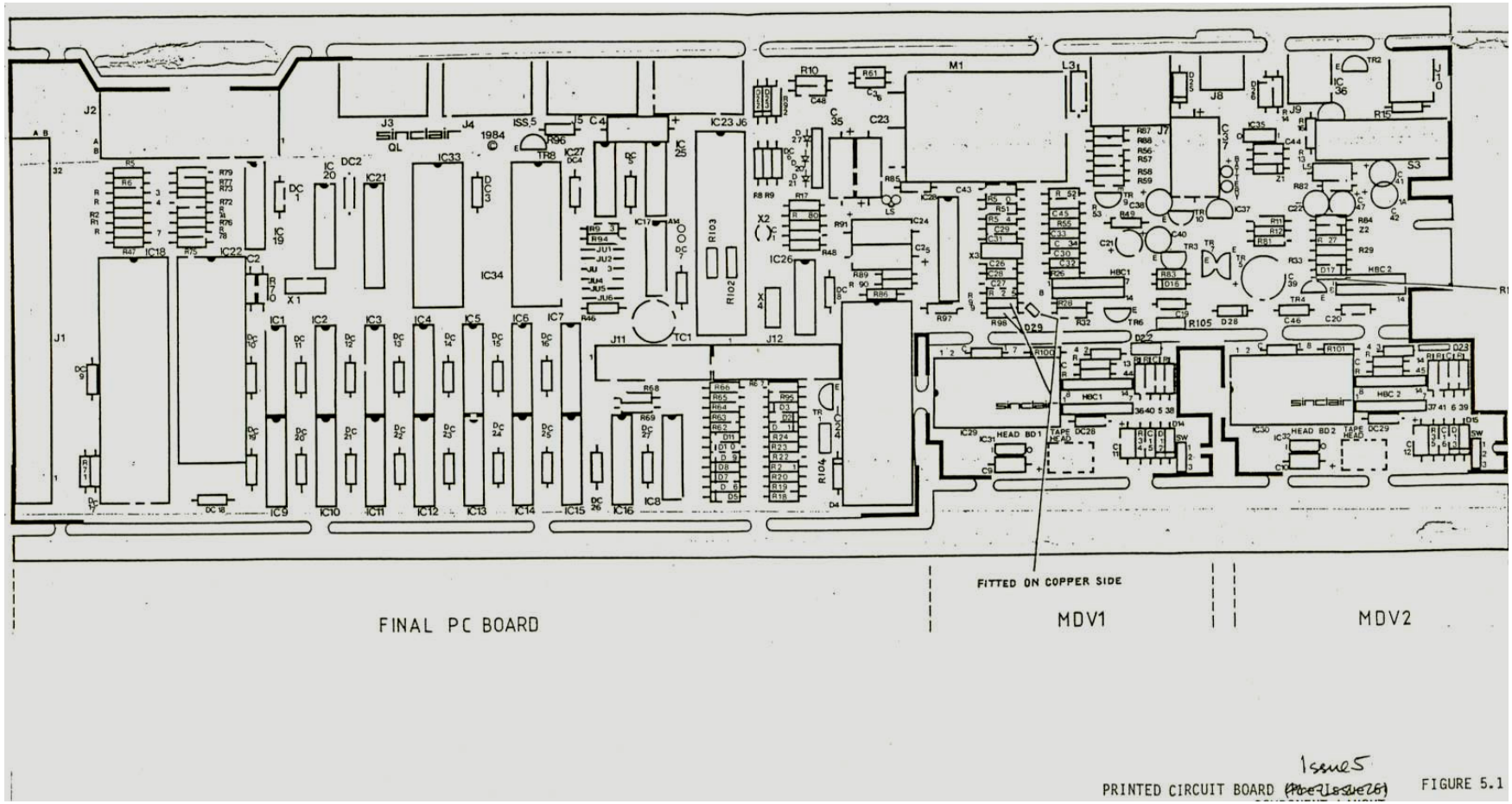
ND IS ARE ONLY FITTED ON SCSI UNITS.







PRINTED CIRCUIT BOARD (Issue 6) FIGURE 5.2
COMPONENT LAYOUT



Issue 5

PRINTED CIRCUIT BOARD ~~(Pre Issue 2)~~ FIGURE 5.1

THOR Professional Computer system.

Main board parts list. November 1986.

Semiconductors.

IC 1.	74 LS 245
IC 2.	74 LS 04
IC 3.	74 LS 74
IC 4.	PAL 16 L 8 Custom logic
IC 5.	74 LS 139
IC 6.	74 LS 04
IC 7.	74 LS 08
IC 8.	74 LS 03
IC 9.	74 LS 113
IC 10.	74 LS 04
IC 11.	74 LS 05
IC 12.	74 ALS 638
IC 13.	PAL 16 L 8 Custom logic
IC 14.	74 LS 245
IC 15.	74 LS 245
IC 16.	74 LS 257 or 258
IC 17.	74 LS 257 or 258
IC 18 to 33 (NEC D-41257 or equivalent)	256K x 1 D-RAM CAS before RAS refresh (MITSUBISHI 41256-15)
IC 34. -15	74 LS 04
IC 35.	74 LS 74
IC 36.	MC 6850 P
IC 37.	MC 6821 P
IC 38.	WD 1772 PH
IC 39.	* MC 146818P * HITACHI HD146818P
IC 40.	74 LS 05
IC 41.	74 LS 03
IC 42.	74 LS 04
Q 1.	MPSA 2369 A
Q 1.	MPSA 2369 A
D 1.	1 N 4148
D 2.	1 N 4148
ZD1	4v3 400mW ZENER DIODE.

Passive components.

R 1.	1 K 1/4 Watt
R 2.	10 K 1/4 Watt
R 3.	150 K 1/4 Watt
R 4.	5 M 6 1/4 Watt
R 5.	150 R 1/4 Watt
R 6.	1 K 1/4 Watt

R 7.	10 K 1/4 Watt
R 8.	10 K 1/4 Watt
R 9.	1 K 1/4 Watt
R 10.	1 K 1/4 Watt
R 11.	1 K 1/4 Watt
RP 1.	8 x 150 Ohm DIL pack
RP 2 to 4.	7 x 1 K SIL pack
Xtal 1.	8.000 MHz HC-18 U
Xtal 2.	32768 Hz watch crystal
C 1.	0.1 Microfarad 30 Volt
C 2.	4 n 7 30 Volt
C 3.	22 Picofarad 30 Volt
C 4.	22 Picofarad 30 Volt
C 5.	0.1 Microfarad 30 Volt
C 6.	0.1 Microfarad 30 Volt
C 7.	* 22 Microfarad Tantalum 16 Volt or 100 Microfarad Electrolytic 16 Volt * NOW 0.1µf ISSUE 4 ONWARDS.
C 8.	0.1 Microfarad 30 Volt
C 9 to C 44	0.1 Microfarad 30 Volt (Decoupling)
NICAD battery	3v6 100 mAH capacity for real-time clock VARTA Mempac or equivalent.

Connectors and sockets.

IC 4.	20 way dil socket
IC 11.	14 way dil socket
IC 12.	20 way dil socket
IC 13.	20 way dil socket
IC 15.	20 way dil socket
IC 36.	24 way dil socket
IC 37.	40 way dil socket
IC 38.	28 way dil socket
IC 39.	24 way dil socket
Keyboard	5 pin 180 degree din PCB mounting socket
Printer	26 way long latch 90 degree ribbon header
Mouse	DB-9 90 degree PCB mounting female plug
Floppy disc	26 way double row PCB pins
SCSI	34 way double row PCB pins
EPROM board	34 way double row 90 degree PCB pins
Expansion	Special 64 way DIN 90 degree PCB mounting male socket with 13 mm pins.
Link board	Special 64 way 90 degree double row pins with 10 mm long tails.
Card guide	Special moulded plastic guide to take single eurocard in expansion socket.
Spacers	M 3 clear by 3 mm long between card-guide and expansion socket.
Screws	self-tapping screws M 3 by 10 mm to fix card-guide to expansion socket.

No.	Item	No. off	Supplier	Ref. No
0	Base	1	Propak)	
1	Front end plate	1	Propak)	
2	Back end plate	1	Propak)	
3	Cover	1	Propak)	
4	Blank panel, full ht.	1	Propak)	
5	Painting	1	Propak)	
6	Feet	4	RS	543-513
7	Screws M3x5 Superdrive	8	D.B.Fasteners	
8	Screws M3x8 Superdrive	4	D.B.Fasteners	
9	Screw self tap 4 x10mm	3	D.B.Fasteners	
10	Screw self tap 4 x 8mm	7	D.B.Fasteners	
11	Screws M3 x 16mm	7	D.B.Fasteners	
12	Screws M3 x 20mm	1	D.B.Fasteners	
13	Screws M3 x 30mm	1	D.B.Fasteners	
14	Screws 6/32 UNC x 25mm	4	D.B.Fasteners	
15	Screws 4/40 UNC x 25mm	8	D.B.Fasteners	
16	Spacers 3mm (metal)	3	Harwin	R2303-14
17	Spacers 8mm (plastic)	6	Verospeed	87-25984E
18	Spacers M3x8mm(metal tap)	1	Verospeed	87-25977J
19	Spacers M3x10mm(metal tap)	1	Verospeed	87-25978E
20	Spacers 18mm (plastic)	8	Verospeed	87-25989G
21	Spacers M3x25.4mm(plastic)	2	RS	543-743
22	M3 nut	8	D.B.Fasteners	
23	Panel anodising	1	Neon Care	
24	THOR panel (screen print)	1	J.G. Printers	

Eprom Board

No.	Item	No. off	Supplier	Ref. No
1	PCB - Eprom	1	Stev. Circuits	
2	34 way Skt. dual row.	1	VSI	DUP76282-417
3	28 way, IC Skt.	6	RR (Bicc-Vero)	681023
4	0.1, 63V Cap	6	RR (E.C.C.)	471004
5	128K EPROM	1	Impulse (NEC)	27128D2
6	256K EPROM	1	Impulse (NEC)	27256D2

Cables & Connections

No.	Item	No. off	Supplier	Ref. No
1	Mains input skt. & switch	1	Belling & Lee	L2724
2	Mains outlet socket	1	RR (Bulgin)	274283
3	Mains lead, 2.5m, fused 5A	1	RR (Bulgin)	274261
4	Mains Supply cable loom	1	RR	
5	DC P.S. cable loom, dual f	1	RR	984107
6	DC P.S. cable loom,Win & f	1	RR	984108
7	34-52way SCSI cable assemb	1	RR	981259
8	26-34way Flop cable assemb	1	RR	981261
9	34-26-34way dual floppy	1	RR	981260
10	2 Amp Fuse 20mm anti surge	1	RR	591058

Additional Modules

No.	Item	No. off	Supplier	Ref. No
1	3.5 inch 720K Floppy	1	PCML	FD 1036A
2	3.5 inch 20Meg Winchester	1	Peripheral Sol.	ROD652
3	'QL' PCB	1	Applied Technology	
4	Power Supply	1	Scource Elec.	

THOR Module

No.	Item	No. off	Supplier	Ref. No
1	PCB Motherboard	1	Stev. Circuits	THOR Mb
2	PCB Con. board	1	Stev. Circuits	THOR Cb
3	64way DIN41612 Skt	1	RR (Bicc-Vero)	685062
4	64 way 90 deg. pins	1	Flair	SPL 118
5	8 way power supply pins	1	RR (Molex)	406034
6	100mm Card guide	1	Conec	ERG 100
7	5 w 180 deg. DIN skt.	1	RS Components	473-278
8	26 way Header long lever	1	RR (Molex)	402025
9	'D' 9 way plug 90 deg.	1	RR (McMurdo)	421125
10	64 way 90 deg. w/w plug	1	RR (Panduit)	299017
11	26 way un. straight header	1)		
12	34 way un. straight header	1)	RR (Molex - 80w)	407154
13	34w 90 deg. un.header	1	Flair	DR250150-34T
14	0.1 63V Caps.	39	RR (E.C.C.)	471004
15	SIL res. 8 pin 1K	3	RR (Kyocera)	3001011
16	DIL res. 16 pin 150R	1	RR (Piher)	057001
17	150R 1/4 W	1	RR (Piher)	PR16 5%
18	1K 1/4 W	5	RR (Piher)	PR16 5%
19	10K 1/4 W	2	RR (Piher)	PR16 5%
18	150K 1/4 W	1	RR (Piher)	PR16 5%
21	1M 1/4 W	1	RR (Piher)	PR16 5%
22	5.6M 1/4 w	1	RR (Piher)	PR15M
23	15pF caps.	2	RR (Mullard)	814119
24	47pF caps.	1	RR (Mullard)	814125
23	100 uF Electrolytic 10 V	1	RR (Dubilier)	342003
26	Crystal 32.768 kHz	1	Davitron	DTFW26
27	Crystal 8.00 MHz	1	Davitron	8 MHz HC1
28	Nick. Cad. Bat. 3.6v	1	RR (Varta)	313157
29	14 way IC skt	1	RR (Bicc-Vero)	681018
30	20 way IC skt.	4	RR (Bicc-Vero)	681021
31	24 way IC skt.	2	RR (Bicc-Vero)	681022
32	28 way IC skt.	1	RR (Bicc-Vero)	681023
33	40 way IC skt.	1	RR (Bicc-Vero)	681024
34	1N4148 Diode	2	RR (Mullard)	801001
35	MPSA 2369	2	RR (Motorola)	444030
36	SN74LS03N	2	RR (Motorola)	432153
37	SN74LS04N	5	RR (Motorola)	432154
38	SN74LS05N	2	RR (Motorola)	432155
39	SN74LS08N	1	RR (Motorola)	432156
40	SN74LS74AN	2	RR (Motorola)	432184
41	SN74LS113AN	1	RR (Motorola)	432200
42	SN74LS139N	1	RR (Motorola)	432211
43	SN74LS245N	3	RR (Motorola)	432249
44	SN74LS258N	2	RR (Motorola)	432326
45	SN74ALS638	1	Online (Texas)	854043
46	MC6821P	1	RR (Motorola)	446127
47	MC6850P	1	RR (Motorola)	446137
48	HD146818AP	1	Impulse(Hitachi)	HD146818P
49	WD1772PH00	1	Pronto	1115442
50	PAL 1 - CST 1.2	1	Online	963025
51	PAL 2 - CST 2.1	1	Online	
52	256K x 1 DRAM	16	Impulse (NEC)	41257C15

Thor Notes V 4.03

Thor Software Status.

18/11/1986
** 4.03 **

SuperBASIC Commands.

CLOCK.

** 4.00 **

The clock now uses a window owned by SuperBASIC, ensuring that it gets displayed in the windowing environment.

EX.

** T.04 **

EX, when invoked from a job other than zero, e.g. when used from a Supercharged program, sets the holding job correctly now. This ensures that sub-jobs go away when the main job completes (or is deleted).

This problem was reported by Helmuth Stuven of Dansoft.

The "option string" parameter, i.e. the one preceded by a semicolon, ** 4.00 **
now accepts an expression, as well as explicit strings and names. This is particularly useful with Xchange, which takes a single numeric parameter for its workspace. For example:

```
EX Xchange; 40
```

would invoke Xchange with 40K workspace. Variables must still be converted to expressions if necessary: this is most neatly done by placing them in parenthesis. The above example is equivalent to:

```
workspace = 40: EX Xchange; (workspace)
```

Previously it was necessary to use the even less obvious form:

```
workspace = 40: EX Xchange; workspace & ""
```

Incidental with this change is the acceptance of numbers by many procedures and procedures which specify a name. This will be appreciated by users of numeric file names; care must be taken to remember that, for example, "SPL 1000000" will attempt to spool a file called "FLP2_1E6" (or "win1_user_1E6" etc)!

EW when invoked from a job other than zero did not wait: now fixed. ** 4.01 **
Complex job structures crashed machine when they set their priorities to zero: now fixed(?). Priority now defined within module (internal change only).

EXTRAS. ** T.05 **
=======

The EXTRAS command now ignores functions and procedures in the Thor roms, as they are conceptually part of the machine and not 'extra'.

HEX$, BIN$. ** T.05 **
==========

HEX$ and BIN$ now accept a single parameter and a second parameter of zero. The effect of both of these is to display the value in the smallest number of digits possible without truncation.

E.g. HEX$(0) = HEX$(0,0) = '0' HEX$(42) = HEX$(42,0) = '2A'
HEX$(-1) = HEX$(-1,0) = 'FFFFFFFF'

BIN$(0) = BIN$(0,0) = '0' BIN$(42) = BIN$(42,0) = '101010'
BIN$(-1) = BIN$(-1,0) = '11111111111111111111111111111111'

The functions previously hung if the second parameter was zero. This bug has never been reported, despite being present in all copies of the QL Toolkit and over 2,000 Q-Discs produced over a 21 month period!

SYS_VARS. ** 4.02 **
========

This is a function (no parameters) to return the address of the system variables. It should be used by all programs that are intended to be portable to later Thor machines.

WCOPY. ** T.04 **
======

WCOPY now copies file headers if either the file-type field or the file-type dependent information field is non-zero. This ensures that only completely plain files are copied without header.

This problem was reported by Talent regarding the copying of TechniQL screen dumps.

WCOPY_F (copy without prompting) and WCOPY_O (copy with overwrite, no prompting) have been added. ** 4.00 **

The prompt message is now in full: "Y/N/A/Q" has now been replaced by "Yes/No/All/Quit".

Much larger buffers are now used to improve performance.

The prompt mess "TO" has been replaced by "=>". ** 4.02 **

WDEL. ** 4.00 **
=====

Extended prompt message: same as WCOPY.

WMON. ** T.14 **
=====

Window £0 is now slightly larger with a black and white checkered border like £1 and £2. This is particularly useful if £1 and £2 have been closed and other jobs are using the screen, as it is much more recognisable.

Window £0 moved down exactly one pixel due to arithmetic error! ** 4.01 **

DEVICES.
=======

BOOT. ** T.06 **
=====

The special device "BOOT" is a read-only device which yields a SuperBASIC in-line file, which attempts to LRUN the file "flpl_boot" or, if unsucessful, the file "winl_boot". It is invoked after the F1/F2 screen, causing the Thor to be booted from a floppy, if present, or the winchester; this sequence ensures that a winchester machine with an eroneous "winl_boot" file can still be booted. The device may be used subsequently by the command:

```
LRUN BOOT
```

Unlike the Q-Disc driver, it does not boot the machine by microdrive emulation and so avoids certain name-clash problems. This has the effect that if microdrives are fitted, or a Q-Disc is fitted in the expansion port, and the built-in bootfiles are not found, these will be used to boot from.

BOOT now performs MRUN rather than LRUN to reduce screen activity. ** 4.00 **

CLOCK. ** 4.01 **
======

If the clock is invalid on reset, no attempt is made to set it to the, probably erroneous, QL clock. Reading the clock can time out if it never 'ticks'. These changes are only of significance in testing.

CON: Keyboard.

** T.10 **

Multi-language keyboards now accepted. Pre-installed are now International, British and Danish. To change between language, type <Alt>-<Sys Req>. This changes to the next in round robbin fashion.

Also changed in this version are the key strokes required for "special" Space and Enter. These are now produced by combination with Ctrl, rather than Shift: this reduces typing errors when typing SEQUENCES OF CAPITALS, without making the rarely used "special" key combinations too obscure.

French and German keyboards added. The French, in particular, is very provisional, until it can be compared with a "standard" french keyboard. ** T.13 **

The Danish version has been slightly modified, allowing the divide symbol to be produced using one of the two key combinations which previously produced c-cedilla.

Greek and Swedish keyboards added. New flag added to allow dual character sets toggled by <Alt>-<Caps Lock>. ** T.14 **

Moving the input channel has been changed to improve the performance of multi-tasking in conjunction with the new window drivers. <Sys Req> now moves to the "next" console channel that is active (it has an enabled cursor flag or is waiting for input), or belongs to a different job, unless that job has another channel which is active. This ensures that even jobs that do not enable their cursor (e.g. Xchange) to be properly multi-tasked. ** T.14 **

<Shift>-<Sys Req> attempts to change to a channel owned by SuperBASIC, if possible with its cursor enabled.

<Ctrl>-<Sys Req> changes to the "next" console regardless of its cursor enabled status.

<Shift>-<Scroll Lock> ("break") now releases the screen lock status. ** 4.00 **

Greek keyboard corrected for lower case ´y´/upsilon translation. Accent keys now accepted in alternate mode. ** 4.01 **

System variables now used for shift keys (sv_shift = $80.w), ctrl key (sv_ctrl = $82.b), alt key (sv_alt = $83.b) and num-lock flag (sv_num = $84.b) status; auto repeat count (sv_arcnt = $90.w) now set to -1 when no key is repeating, allowing a non-destructive test for key press together with the auto repeat buffer (sv_arbuf = $8a.w).

Console channels are now opened BEFORE the active one. This ensures that the keyboard will return from a job to its originator unless the user explicitly changes windows using the <Sys Req> key or other jobs preempt control of the screen. This means that jobs "stack" in a fairly intuitive manner. ** 4.01 **

German keyboard fixed to have one double-s ("beta") and one plus key, instead of two plusses! ** 4.02 **

Greek keyboard fixed to get accent key right. ** 4.02 **

<Sys Req> now changes screen in scheduler loop to prevent clashes. ** 4.02 **

The keyboard definition table pointer, sv_kbd, has been changed to $150, to ensure long word alignment (for Thor-20). This should not cause any problems as this was not previously documented. The "raw" keyboard queue is now pointed to by sv_kbdq ($154), allowing improved keyboard response to be provided by "greedy" device drivers, such as the floppy, which need to hold off interrupts for significant periods. ** 4.02 **

Window changes on <Sys Req> are now done in the scheduler loop to prevent window mixing. ** 4.02 **

Greek keyboard finalised: in greek mode, the <`> key is special: when it is pressed, nothing is output, but if any of the lower case keys <a>,<e>,<h>,<i>,<o>,<y>,<v> (alpha,epsilon,eta,iota,omicron,upsilon,omega) immediately follow it, they are converted to their accented (dotted) form. <Shift>-<`> produces a double accented upsilon. ** 4.03 **

PAR. ** T.09 **
====

All options are now recognised:

```
PAR[N|C|R][_bufsize][K]
```

Options:

Newline translation:

- N - Newline: <newline> => CR LF (default).
- C - Carriage return: <newline> => CR.
- R - Raw.

Buffer size = 128 if neither <bufsize> or K present;
= <bufsize>, multiplied by 1024 if K present;
= 1024, if only K present.

Once a channel has been closed, a further channel may be opened, even if output is still occurring. Therefore to perform background printing from memory, open a channel with a buffer size adequate for the entire output: the output will apparently complete immediately, and further printer output may be initiated. Note that it is the responsibility of the printing job to ensure that memory is not "hogged": a channel occupies about 100 bytes more than the buffer size specified.

Except in raw mode, a page throw is added at end of file if not already present.

The parallel port now checks for the present of TRA vectors for output translation. This is not performed on "raw" channels ("parr").

Interrupts enabled, to enable maximum output speed when using printers faster than 50 cps. ** T.12 **

Bug fixed, which could cause a system crash when using TRAnslated characters when the output buffer is full. ** T.14 **

Screen Driver (SCR). ** T.14 **

Full dynamic windowing has been added. Each job is allocated a buffer area for its windows. This area is a rectangle which encloses all the windows which are owned by the job, plus all area of the screen which have been previously occupied by windows owned by the job that have been written to. This means that windows that are opened and immediately redefined, as is done by the UT.CON and UT.SCR vectored routines, do not contribute to the buffer space area. Otherwise, buffer area do not shrink, which ensures that top line banners etc remain with the job. The exception to this is SuperBASIC, allowing the use to reduce it from using the entire screen.

The driver only allows buffer areas which are unobscured to be written to, all others being preserved. Attempting to perform a write to such an area will return "not complete" if finite a timeout is specified or wait until unobscured. Areas may be rendered writable by issuing an SD.TOPW ($3a) i/o trap on any screen or console channel belonging to the job, or moving the flashing cursor to a console window belonging to the job (See the description of CON for enhanced cursor moving). When a window is first opened, the job´s buffer area is made writeable: this means that a new job overlapping SuperBASIC´s area (normally all of the screen!) will suspend SuperBASIC unless the cursor is specifically moved back; thus, it is sensible to always use EX (manually) rather than EW.

Closing all the windows belong to a job will release its buffer area: this should therefore not be done unless this effect is desired; for example, this may be used when it is desired to "really" move or shrink a window area.

Windowing now can be turned off (for compatability with a minority of irregular programs) by setting the byte sv_nowin (offset $85) in the system variables; for example: ** 4.03 **

```
POKE SYS_VARS+133, 255
```

This will only affect jobs opening their first windows with the flag set; to remove a job´s (e.g. SuperBASIC´s) window buffer, close all of it´s windows and reopen them.

Watermark. ** T.08 **

Installed in Winchester only: currently in second top rom only!

Installed in RAM drive. ** T.11 **

Installed in FLP driver. ** T.13 **

Now in correct rom. ** 4.00 **

SUMMARY OF VERSIONS.

T.04:	EX	Bug fix (owner job).	9/ 9/1986.
	WCOPY	Bug fix (non-plain file headers).	
T.05:	BIN$	Bug fix (0 bits). Now accepts value only.	10/ 9/1986.
	EXTRAS	Now ignores Thor roms.	
	HEX$	Bug fix (0 bits). Now accepts value only.	
T.06:	BOOT	Device added.	10/ 9/1986.
T.07:	WIN	Various enhancements.	12/ 9/1986.
T.08:	WIN	Watermark Added (winchester only).	19/ 9/1986.
T.09:	PAR	First complete version.	15/ 9/1986.
T.10:	CON	Multi-language keyboard support.	19/ 9/1986.
T.11:	RAM	Relinked to include watermark.	19/ 9/1986.
T.12:	NFS	Linked in.	22/ 9/1986.
	PAR	Performance improved with fast printers.	
	WIN	Not installed if Pal absent.	
T.13:	CON	French, German keyboards added; Danish improved	22/ 9/1986.
	FLP	Now includes watermark. Re-arrangement of roms.	
T.14:	CON	Greek (HELLAS), Swedish keyboards added.	10/10/1986.
	CON	<Sys Req> response improved.	
	PAR	TRA bug fixed.	
	SCR	Full windowing version.	

Thor Notes V 4.03

4.00:	Thor	First full release version.	12/10/1986.
	BOOT	Screen clears reduced.	
	CLOCK	(procedure) New window for windowing software.	
	CON	Further <Sys Req> and <Scroll Lock> improvements.	
	EX	Enhanced option string input.	
	FSDs	Watermark moved to correct rom.	
	WCOPY	New entries added; improved messages; large buffers.	
	WDEL	Improved messages.	
4.01:	CLOCK	(device) Error handling improved.	28/10/1986.
	CON	Greek keyboard enhanced; improved system interface.	
	CON	Job stacking improved.	
	EX	Various bug fixes.	
4.02:	CON	Greek & German kbds fixed; Sys_req improved.	16/11/1986.
	SYS_VARS function added.		
	WCOPY	"TO" replaced by "=>".	
4.03:	CON	Greek (HELLAS) keyboard changed again.	18/11/1986.
	SCR	System variable to disable windowing.	

EPROM BASED $F0000 upwards.

HARDWARE INTERFACING:

1) RAM: 640K
   System stack at HIMEM - 1K

2) FLOPPY: (~~FLP~~ FLP1_, FLP2_)
   QDisc based system from QJUMP / TONY TEBBY.
   ADAPTED for Thor h/w.
   "EXTRAS" included in Thor system.

3) WINCHESTER (WIN1_)
   BASED on CST SCSI system, RELATED to QDISC: Interrupt Dri
   HEIRARCHICAL DIRECTORIES: FS.MKDIR : MAKE_DIR (SB).
   DATE STAMPING; BACKUP / ACCESS / MODIFIED DATES: FS.DATE.

4) CLOCK
   SET_CLOCK COMMAND, gets 'QL' CLOCK. - copies it To B.B. clock.
   READ AT POWER UP, COPIED to 'QL' CLOCK.

5) PRINTER PORT
   DEVICE Name 'PAR' = 'PARN' - Newline → <CR> <LF> } <FF> at end of file
   'PARC' = Newline → <CR>
   'PARR' = Raw (Untranslated).
   'PAR_5' = 5K buffer etc.
   _N adds N K Bytes for buffer space.
   Supports TRA command except when Raw mode. MG only?

6) MOUSE PORT
   6821 PORT : Interrupt Driven. Heavily dependant on windowing software.
   No OS Support YET : CURRENTLY only ICE.

7) KEYBOARD
   6850 PORT : Interrupt Driven : Interaction with floppy?
   KEYROW PROBLEM.
   FUNCTION KEYS & NUMERIC PAD.
   LEDS.
   LANGUAGES. (ERROR MESSAGES IN MG ROMS): LOADABLE.
   PRINT SCREEN — QDUMP.

TOOLKIT II : QJUMP / TONY TEBBY DESIGN.

SOFTWARE OS FEATURES

1) RAM DRIVE 'RAM1_' to 'RAM8_'

CST DESIGN : FASTEST SCREEN LOAD AROUND.

BUFFERING REWRITE FOR 4.10: COPY now TWICE as FAST.

2) WINDOWING

AUTOMATIC "SWAPPING" between JOBS.

SYS REQ key.

SD.TOPW call.

Flag in system Variables to turn off (V 4.0B): SV.NoWin ($85)

3) WATERMARK

FS.WATER call.

Fields are currently "THOR", serial number (binary).

stored "shadowed" under hardware.

SUPER BASIC

1) EX, EW

OWNERSHIP of JOBS FIXED.

NUMERIC parameters: EX XCHANGE ; 100

2) SYS_VARS

Returns address of SYSTEM VARIABLES.

Allows portability to THOR-20 ---

3) CLOCK

Only one clock JOB

Channel owned by (CALLING JOB #); active when BASIC is.

4) WCOPY

FASTER.

WCOPY_O/-F.

'=2' instead of 'TO' (4.02)

'Yes/No/All/Quit' instead of 'Y/N/A/Q' - ALSO WDEL.

5) HEX$, BIN$

LENGTH now optional : HEX$(256) = "100"
HEX$(-1) = "FFFFFFFF"

4) BOOT

LOADS FLOPPY or Winchester BOOT file.

COULD BE MODIFIED.

APPLICATIONS

XCHANGE 3·84

1) TASKS
2) QUILL: MAIL-MERGE
   GLOSSARIES
3) ARCHIVE: BUG FIXES ETC.
4) EASEL: 3D BARS; PLOTTERS
5) ABACUS: GOAL SEEK.
6) XCHANGE IM/~~EX~~ EX-PORT
7) ~~TSL~~
8) Installation & Configuration.

ICE

1) REWRITTEN in PART.
2) GRADUALLY INCORPORATING LOW LEVEL FUNCTIONS in O/S
3) MOUSE / CURSOR KEYS.
4) USER VISIBLE CHANGES NEEDED:-
   CALCULATOR numeric input.
   HEIRARCHICAL DIRECTORY support.
   O/S Driven mouse.

QDUMP

1) REWRITTEN ~~for~~ THOR.
2) Default DIRECTORIES etc.
3) FILE STRUCTURE.

DMU

FILED

DISCED

BACKUP

CONVERT

HP / GLASS PENDULUM.

Set Primary Addressing Mode Only

Previously, the interface always required a secondary address in the range of 0 to 5 when used as a device. It is now possible to configure the system to respond to a primary address only. This has been implemented to allow easier use of the BBC machine as a device with other controllers that cannot easily send secondary addresses. For example, programs can be simply listed across from an HP85 by using its **PRINTER IS n** command.

Primary addressing only is selected by prepending the character "P" to the device address. This is an alternative to the mode of use with secondary addressing selected by ***IEEE n** whose use remains unchanged. (Refer to the manual pages 5-17 to 5-19, and 7-37 to 7-41.) The syntax is:

***IEEE Pn** ("n" is the primary address, 0...30.)

If a secondary address is sent, it will be ignored; i.e. in effect, all I/O is to what is called secondary address zero in the alternative mode.

IMPORTANT: Please note that you are not permitted to sw between the forms ***IEEE Pn** and ***IEEE n** unless there is an intervening **<BREAK>**. For example:

```
(Incorrect)          (Correct)
*IEEE P6             *IEEE P6
....                 ....
*IEEE 3              <BREAK>
                     ....
                     *IEEE 3
```

The following examples illustrate the two functionally equivalent approaches to sending the string "Hello" from a controller BBC micro to one at device address 3:

Using primary addressing only:

```
(Controller)                    (Device)
10 *IEEE                        10 *IEEE P3
20out_chan =OPENOUT"R3"         20 in_chan = OPENIN"R"
30 PRINT £out_chan,"Hello"      30 INPUT £in_chan, string$
                                40 PRINT string$
```

Alternatively, with secondary addressing:

```
(Controller)                    (Device)
10 *IEEE                        10 *IEEE 3
20out_chan =OPENOUT"R3,0"       20 in_chan = OPENIN"R"
30 PRINT £out_chan,"Hello"      30 INPUT £in_chan, string$
                                40 PRINT string$
```

This transaction will fail at the last step because the hard entry will detect REN and give the error "Controller on bus". The problem is easily resolved by making a soft entry instead:

```
*IEEE 8
```

then take control unconditionally with:

```
*CON
```

You will have to exercise care to avoid multiple controllers, should the system controller re-enter the IEEE filing system with ***IEEE.** A safer technique would be to pass control from the system controller to the device with ***TCT n.** (Refer to examples in Section 2.)

1.1.7 Reading Previous *OPT Values

The previous value of the ***OPT** calls **0** to **10** can be read back.

***OPT** calls are synonymous with OSBYTE call 139. When such a call is made from an assembly language routine (or via the BASIC function **USR(&FFF4)**) with the X register in the range 0 - 10, then the Y register returns with the previously set value.

The feature has been added so that programmers can preserve the options currently in effect should they wish to make any changes from, say, within an interrupt routine.

The example is an assembler version of ***OPT 7,32** which will set the first character used to terminate output strings to the **<SPACE>** character, 32. The character previously used (by default, 13) is saved in the location **old_value:**

```
...
LDA £139
LDX £7
LDY £32
JSR &FFF4              (OSBYTE call *OPT 7,32)
STY old_value          (Save previous value from Y)
...
```

If the code is run a second time, **old_value** will contain the **<SPACE>** character, 32.

Recasting this as an equivalent BBCBASIC program:

```
10 A% = 139
20 X% = 7
30 Y% = 32
40 old_value = (USR(&FFF4) AND &FF0000) DIV &10000
50 PRINT old_value
```

1.2.3 Hanging for "Byte In" (Fixed 1.97)

Data transfers on the lines of the following example will "hang" after a number of iterations:

(Controller)
```
10 *IEEE
20 out_chan=OPENOUT"R4,0"
30 REPEAT
40   PRINT £out_chan,"Hello"
50   TIME=0
60   REPEAT: UNTIL TIME>200
70 UNTIL FALSE
```

(Device)
```
10 *IEEE 4
20 in_chan=OPENIN"R"
30 REPEAT
40   INPUT £in_chan,string$
50 UNTIL FALSE
```

The device program is run first to avoid bug (1.2.1) and also to set the device primary address to 4 before any addressing takes place.

The problem arises whenever the device machine is waiting for "Byte In" whilst the other is attempting to send a secondary address. If this is likely to bother you, and an upgrade to 1.97 is not available, use primary addressing mode only on the device machine. The example becomes:

(Controller)
```
10 *IEEE
20 out_chan=OPENOUT"R4"
30 ...etc.
```

(Device)
```
10 *IEEE P4
20 in_chan=OPENIN"R"
30 ...etc.
```

1.2.4 Hanging during a *LOAD/*SAVE Transfer (Not fixed)

This problem very rarely arises. The explanation is similar to (1.2.3), and if you use primary addressing mode it will not occur.

1.2.5 Entering Device Mode through a Soft Key (Fixed 1.98)

The following sequence illustrates the bug:

```
*KEY 0*IEEE 5|M
*FX 138,0,128
```

- the system hangs after the soft key expansion. However, if you experiment with other valid primary addresses in the range 0 to 30, roughly half work and half fail. The problem has been traced to a simple coding error. If you use this sort of trick for remotely driving a device machine from the OSCLI secondary address, avoid the problem by choosing an address that works, e.g. 6.

5 Re-interrupting OSCLI Calls (Not fixed)

Strictly, this is not a bug but simply something that you will have to bear in mind should you make several calls in rapid succession to the OSCLI secondary address. For example, the following does not work:

```
(First, on the device)
*IEEE 6

(Second, on the controller)
10 *IEEE
20 oscli=OPENOUT"R6,1"
30 PRINT £oscli, "KEY 0MODE 7^M*DISC^M*CAT^M*IEEE 6^M"
40 PRINT £oscli, "FX138,0,128"
```

A problem occurs when line 40 interrupts the processing in the device machine of line 30. The cure is to insert a brief delay at line 35:

```
35 A%=INKEY(10)
```

As a general point, if you encounter difficulties using the device secondary addresses, try inserting a few judicious delays.

7 Spurious Byte with the OSCLI *SAVE (Not fixed)

Continuing the example in (1.2.6):

```
50 A%=INKEY(400)          (Allows completion of *CAT)
60 PRINT £oscli, "SAVE """" 7C00 7FFF"
70 MODE 7
80 *LOAD 6,0 7C00
90 CLOSE £oscli
```

A copy of the device machine|s screen complete with a catalogue of its disc should be displayed on the controller. Unfortunately, a spurious first byte is sent by the ***SAVE** so that the screens are not in register. If you really have to use this sort of transfer, you will need to fiddle the OSCLI command to ***SAVE "" 7C01 8000** to strip the rogue byte.

This fault only shows if a call is made to ***SAVE** from the OSCLI secondary address: it does not affect transfers typed in at the keyboard. Since the root of the problem is as yet unknown, it may well appear in other guises.

THOR Technical note 1. 16/12/86.

Using external Microdrives with the THOR.

It has come to our attention that several methods exist for the incorporation of external microdrives with the THOR computer system, and this technical note is intended to standardise the installation procedure.

Firstly it should be understood that the selection of microdrives is carried out by sending a train of pulses from the IPC device, to the first microdrive position on the QL board, this device then actively responds by re-transmitting the pulse train to the next device, and so on to the last device in the chain. Each device is identical, and removes one pulse from the train, until the desired device receives only one pulse.

It is necessary to link the pulse across the missing microdrive positions on the QL board, to allow the external drives to be found. A connection should be made between pins 1 and 2 of each microdrive connector to do this. These are the nearest pins to the IPC on the board, and can be linked with a short u-shaped piece of tinned copper wire pushed into the turned-pin socket strip.

The standard microdrive is powered from the 9 Volt rail of the QL, which is no longer present. It is therefore necessary to provide a supply in another way, and we suggest that a 27 Ohm series resistor (1/2 Watt rating) should be fitted in series with the existing inductor L5, to carry power from the 12 Volt rail (accessible at the position of the 78L12 voltage regulator IC 37, now removed). To do this, it is necessary to lift the end of L5 which previously connected to the 9 Volt rail from the QL circuit board, and to join this free end to the resistor. Care should be taken to use sleeving to insulate this floating connection, and to leave the leads of the components as short as possible.

THis modification should allow external cased microdrives (typically the type intended for the Spectrum) to function identically to those originally fitted to the QL. However it may be found that those supplied for the Spectrum are often to a lower specification than the QL parts, and may format to a reduced capacity. It is unlikely that anyone would want to use these drives to save data, and they will normally read existing QL cartridges without difficulty.

Graham Priestley.

THOR Service Manager.

THOR Technical note 1. 16/12/86.

Using external Microdrives with the THOR.

The THOR system as supplied uses floppy discs as the basic data-storage medium, however it is still possible to connect external microdrives if certain modifications are made, and this technical note is intended to standardise the installation procedure.

Firstly it should be understood that the selection of microdrives is carried out by sending a train of pulses from the IPC device, to the first microdrive position on the QL board, this device then actively responds by re-transmitting the pulse train to the next device, and so on to the last device in the chain. Each device is identical, and removes one pulse from the train, until the desired device receives only one pulse.

It is necessary to link the pulse across the missing microdrive positions on the QL board, to allow the external drives to be found. A connection should be made between pins 1 and 2 of each microdrive connector to do this. These are the nearest pins to the IPC on the board, and can be linked with a short u-shaped piece of tinned copper wire pushed into the turned-pin socket strip.

The standard microdrive is powered from the 9 Volt rail of the QL, which is no longer present. It is therefore necessary to provide a supply in another way, and we suggest that a 15 Ohm series resistor (1/2 Watt rating) should be fitted in series with the existing inductor L5, to carry power from the 12 Volt rail (accessible at the position of the 78L12 voltage regulator IC 37, now removed). To do this, it is necessary to lift the end of L5 which previously connected to the 9 Volt rail from the QL circuit board, and to join this free end to the resistor. Care should be taken to use sleeving to insulate this floating connection, and to leave the leads of the components as short as possible.

This modification should allow external cased microdrives (typically the type intended for the Spectrum) to function identically to those originally fitted to the QL. However it may be found that those supplied for the Spectrum are often to a lower specification than the QL parts, and may format to a reduced capacity. It is unlikely that anyone would want to use these drives to save data, and they will normally read existing QL cartridges without difficulty.

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